SEIMI: Efficient and Secure SMAP-Enabled Intra-process Memory Isolation

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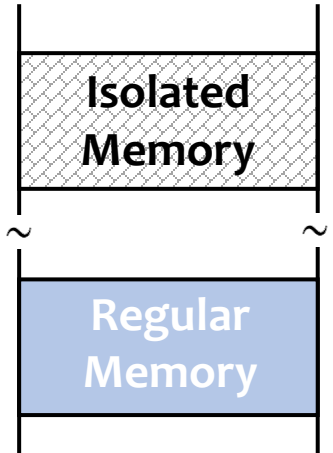

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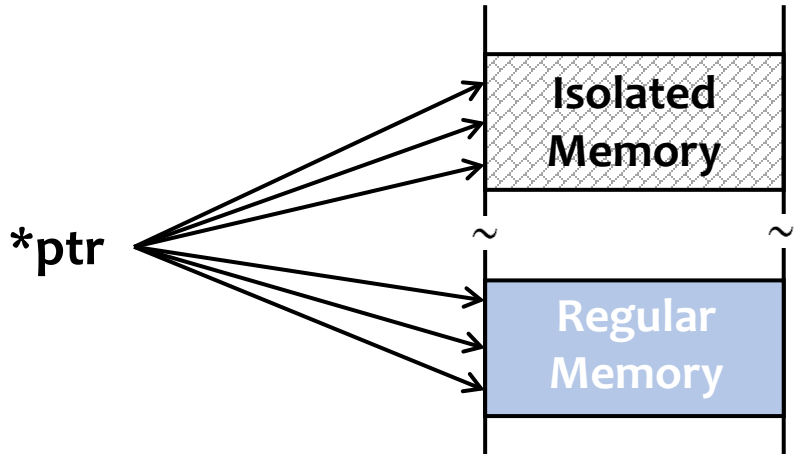

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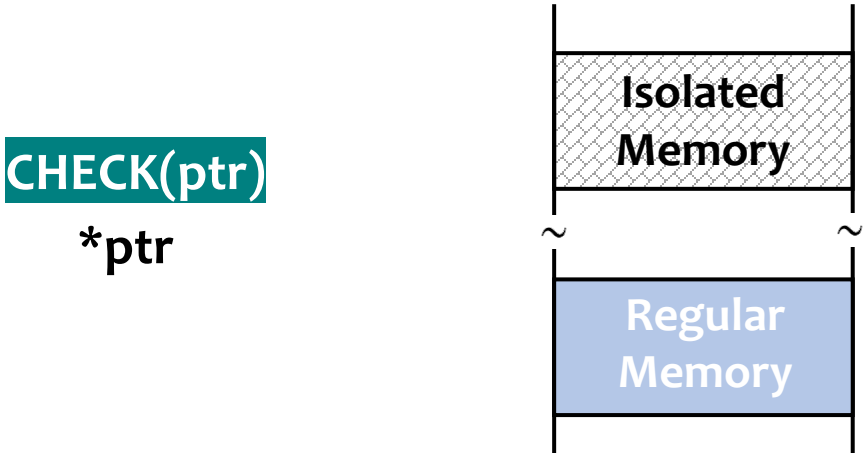

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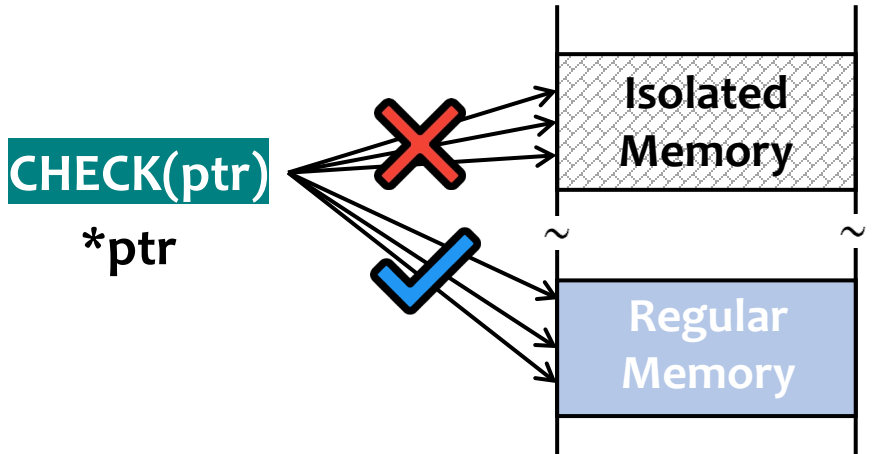

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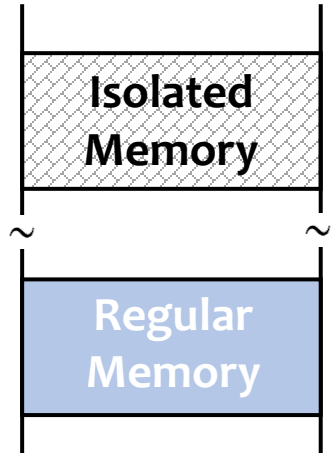

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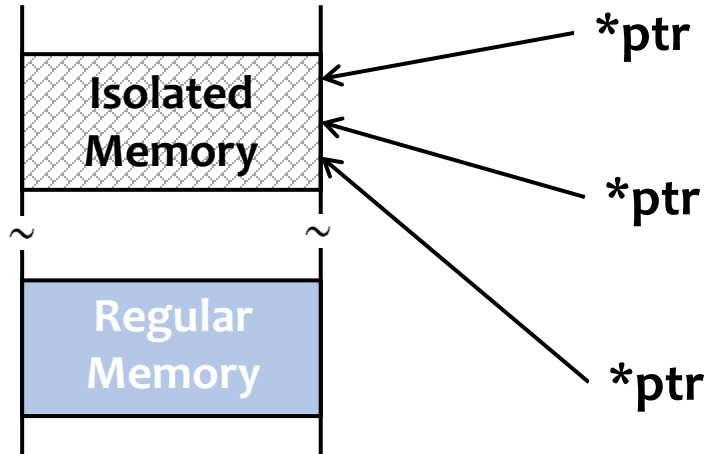

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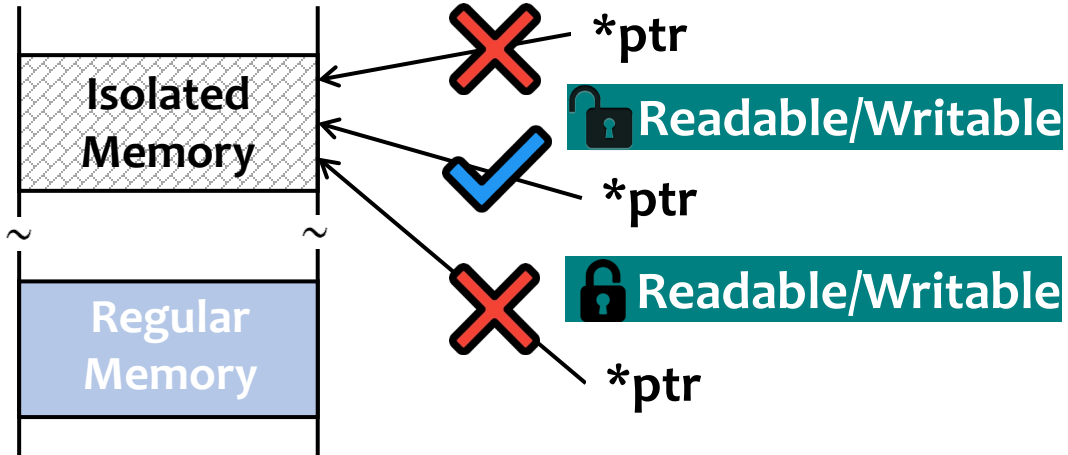

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But they are not efficient enough as we expect.

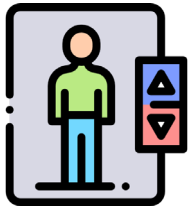
Threat Model

- **We consider a defense that protects a vulnerable application against memory corruption attacks.**
  - Web servers, databases or browsers.

- **The design of this defense is secure:**
  - Breaking memory isolation is a prerequisite for compromising the defense (e.g., attackers cannot hijack the control flow before it).

- **Attackers' capabilities:**
  - Arbitrary read and write by exploiting memory corruption vulnerabilities.

Outline



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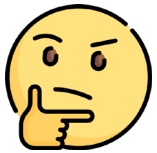

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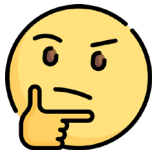

Is there a privileged hardware feature which is more efficient than Intel MPX/MPK for the memory isolation ???

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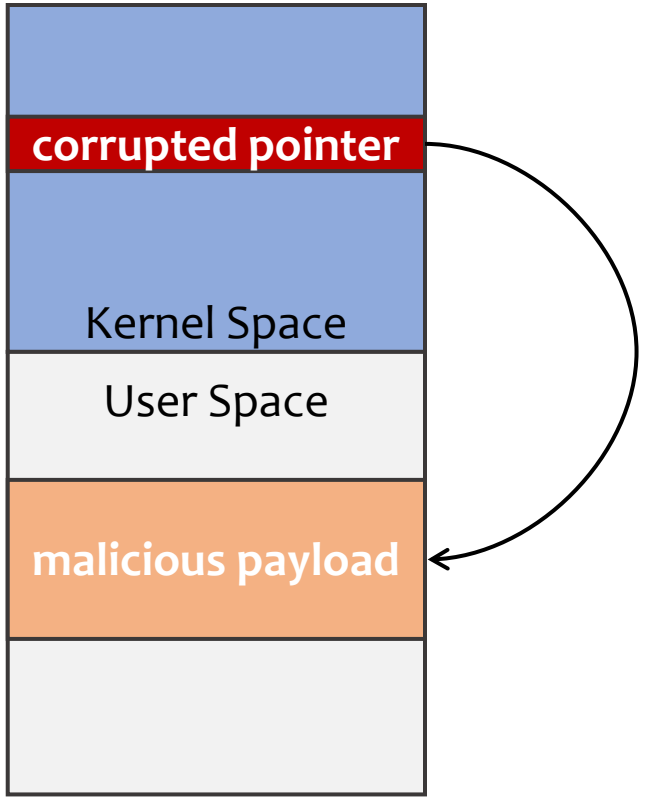

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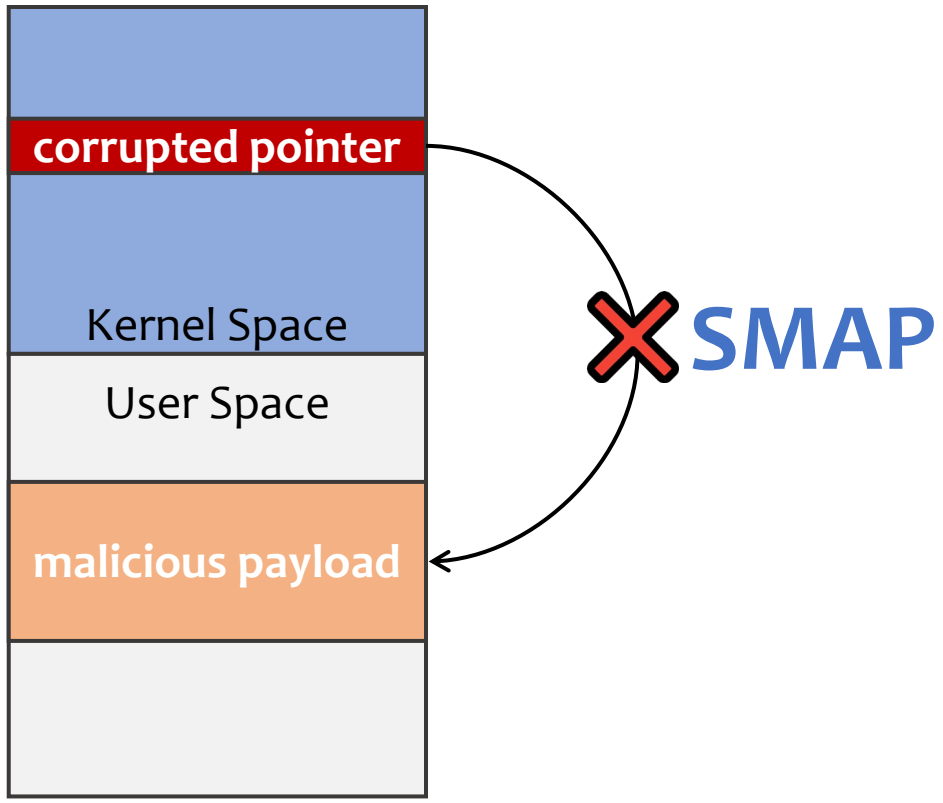
- Intel and AMD provide the **Supervisor-mode Access Prevention (SMAP)** hardware feature to disable the kernel access to the user space memory.



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Intel SMAP is more efficient than Intel MPK for controlling memory access permission.

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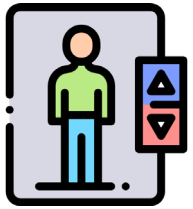

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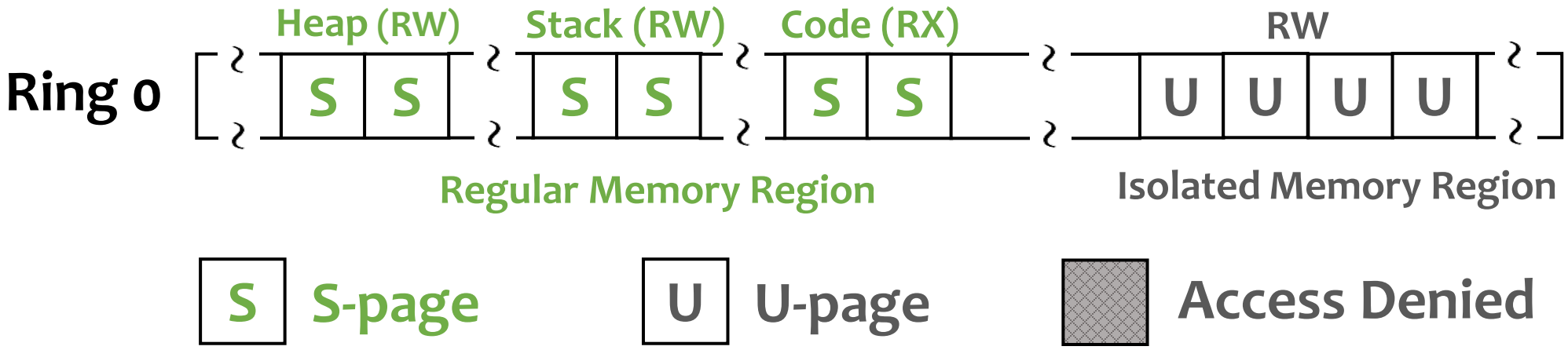

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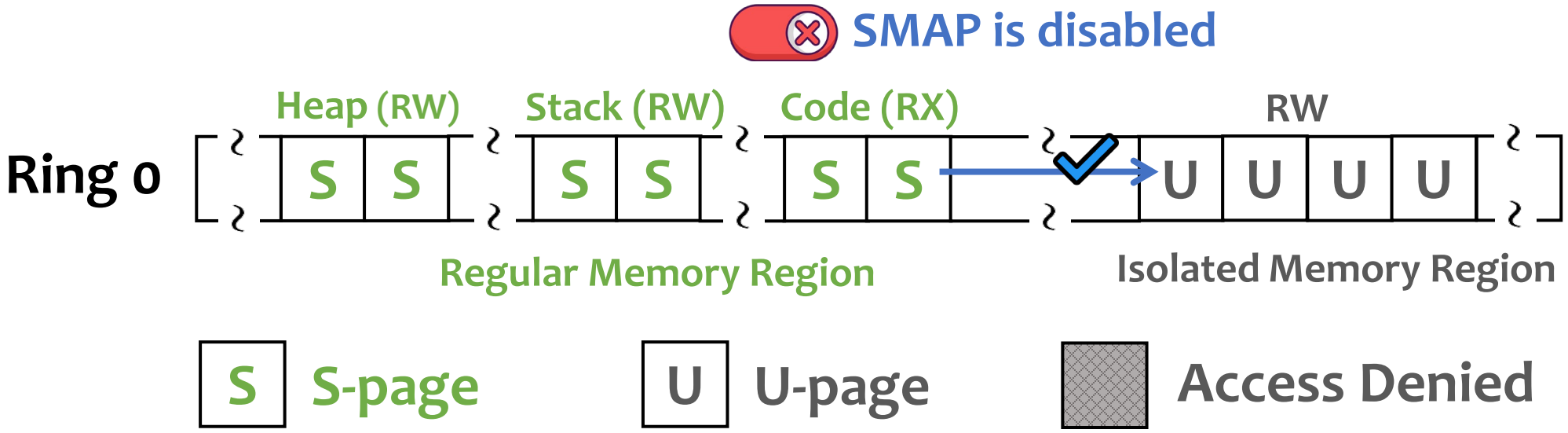

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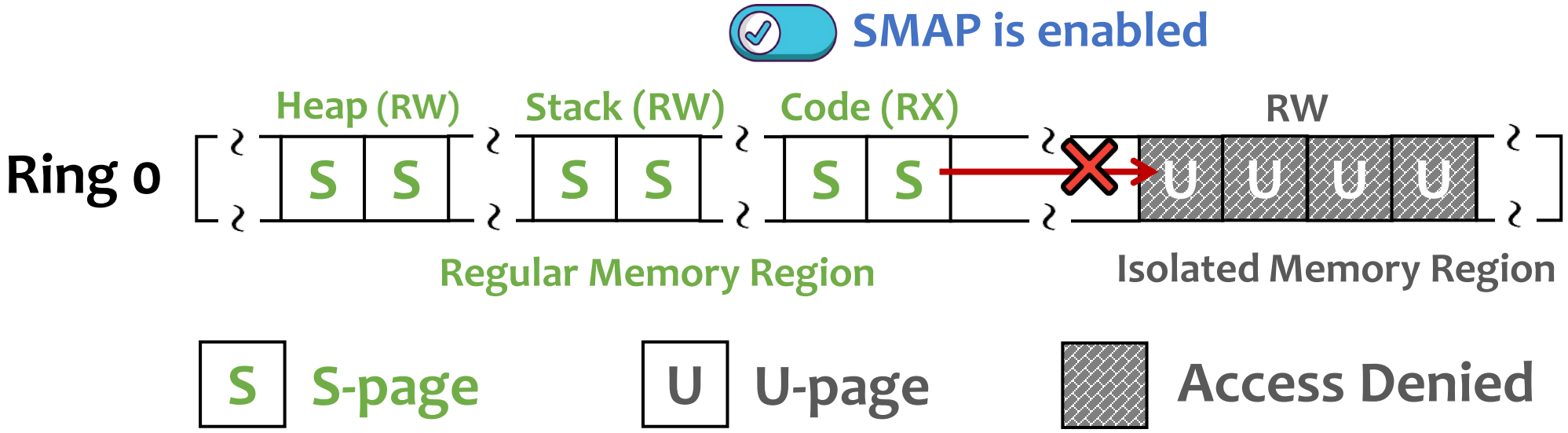

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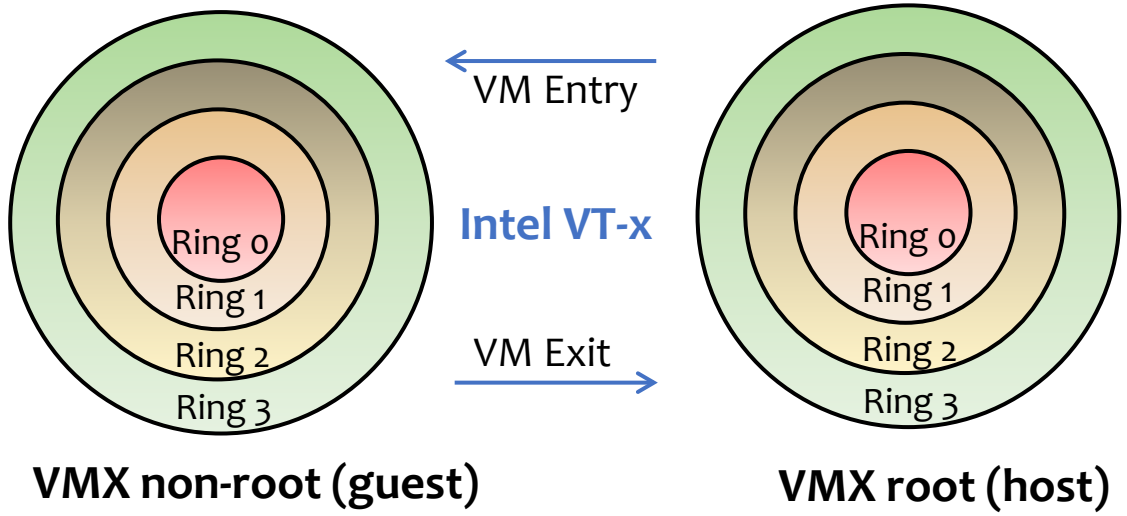

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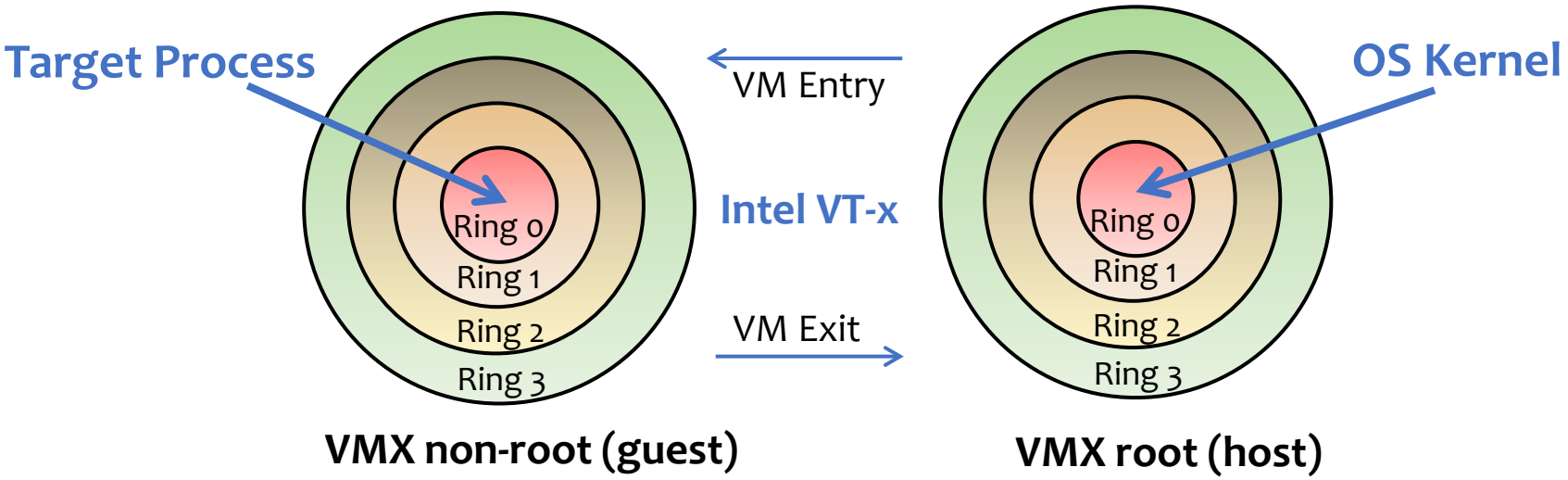

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- **C-3: Preventing the abusing of the privileged hardware features.**
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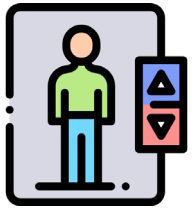

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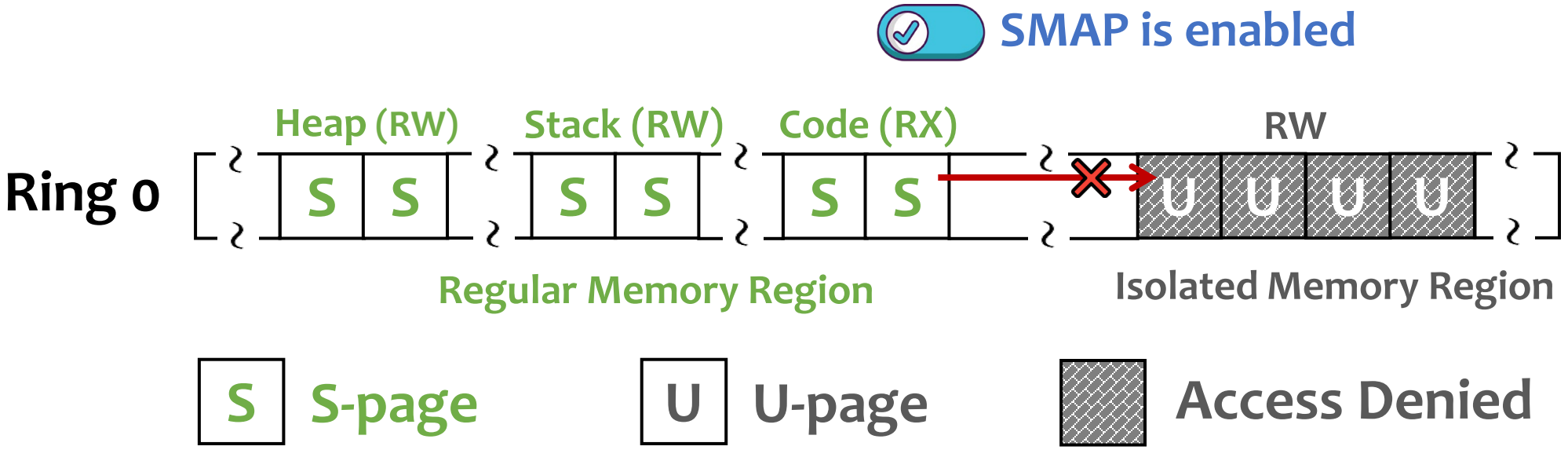

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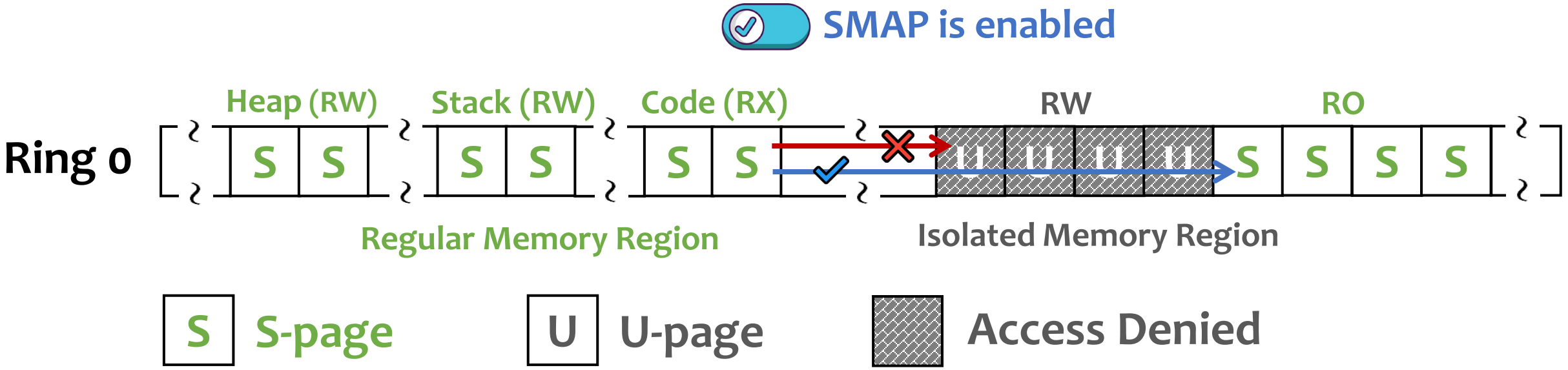

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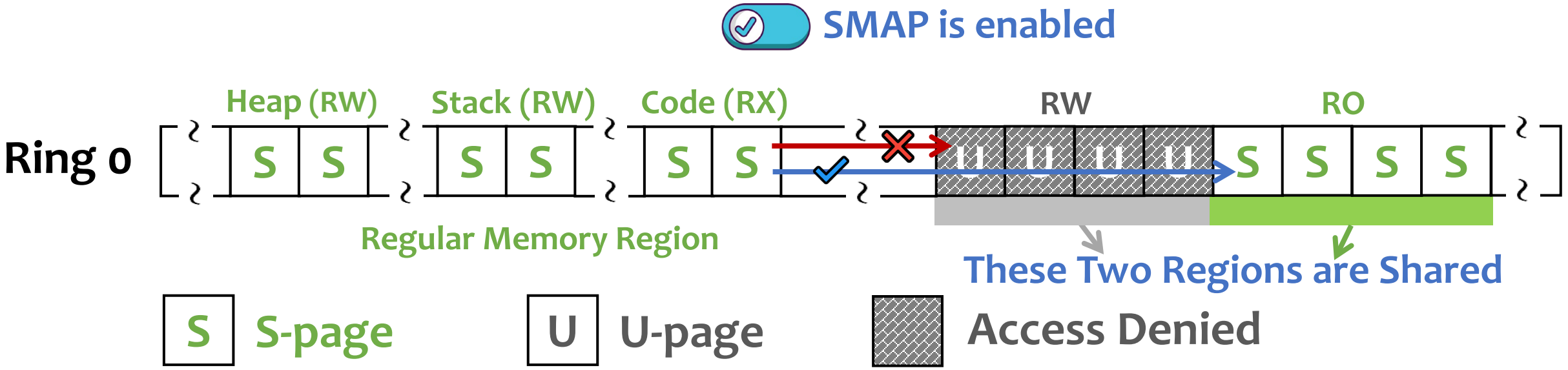

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- **Solution:**

  - Placing the privileged data structures and their operations **into the VMX root mode**.
  - We leverage the Intel VT-x technique to force all these events to **trigger VM exits** and enter into the VMX root mode.

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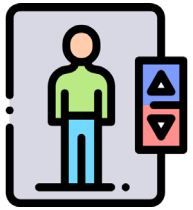

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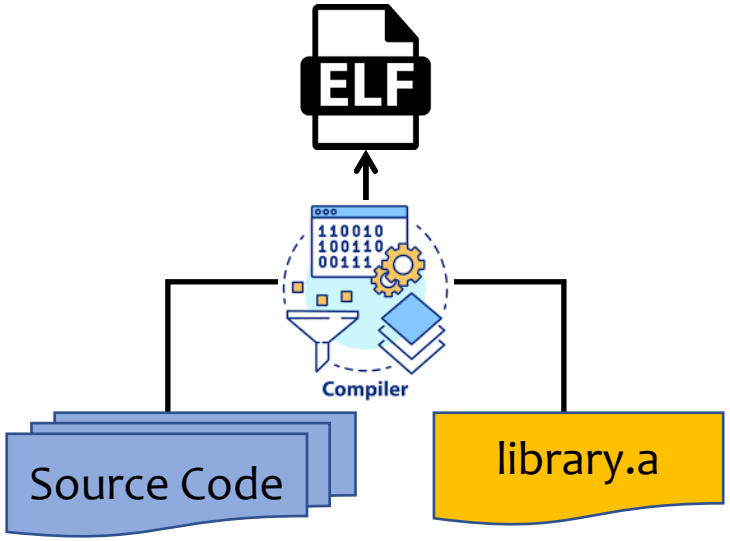

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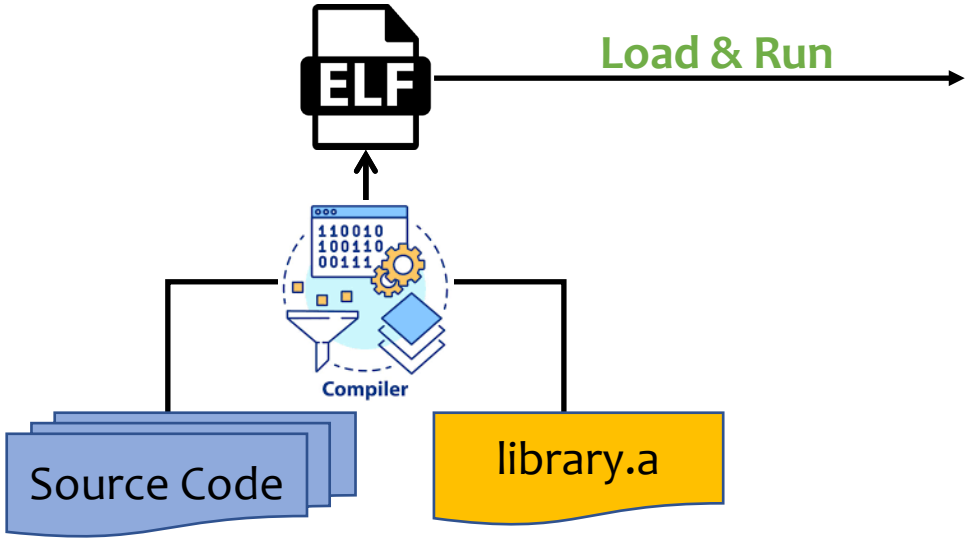

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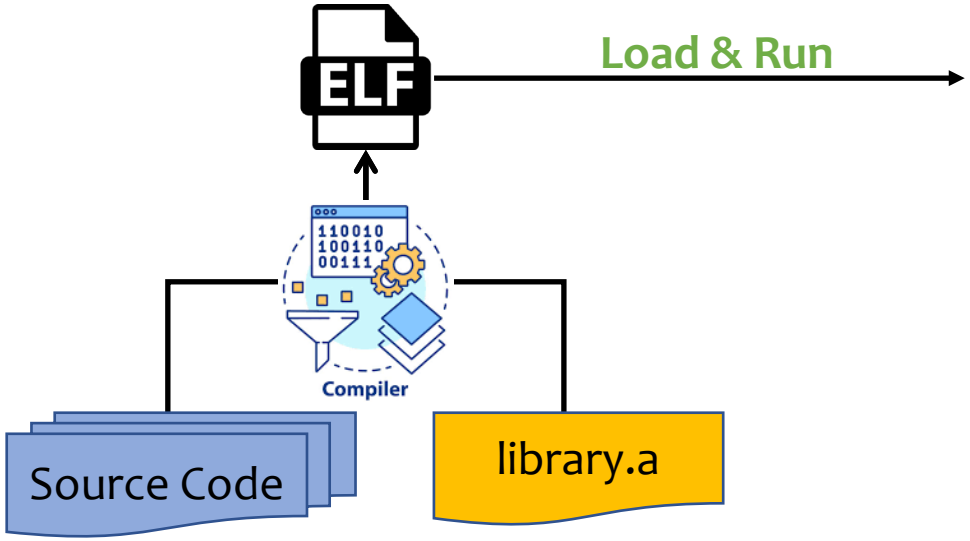
- **SEIMI is implemented on Linux/X86_64 platform.**
- **Two Phases in SEIMI —— Compilation Phase and Runtime Phase**



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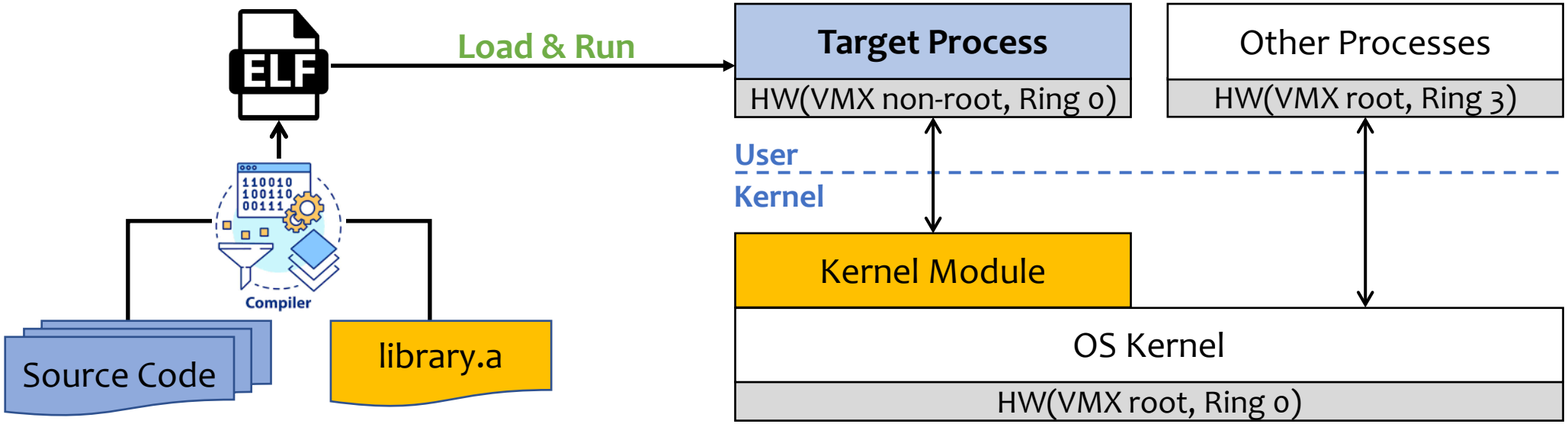

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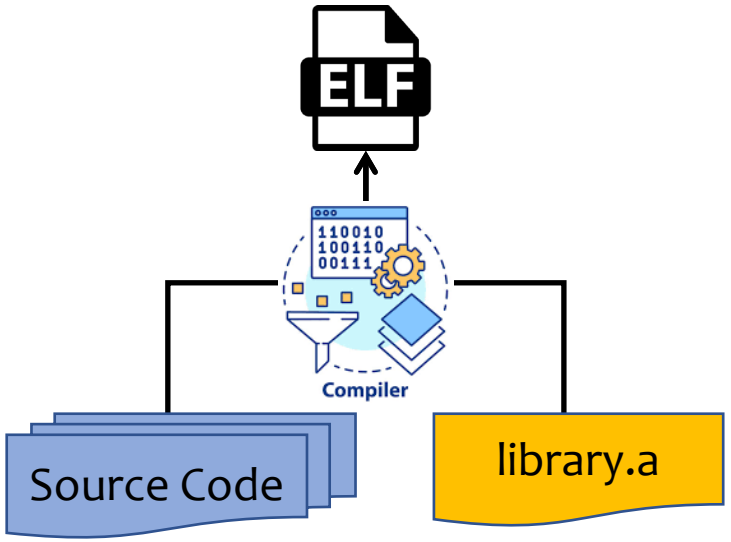

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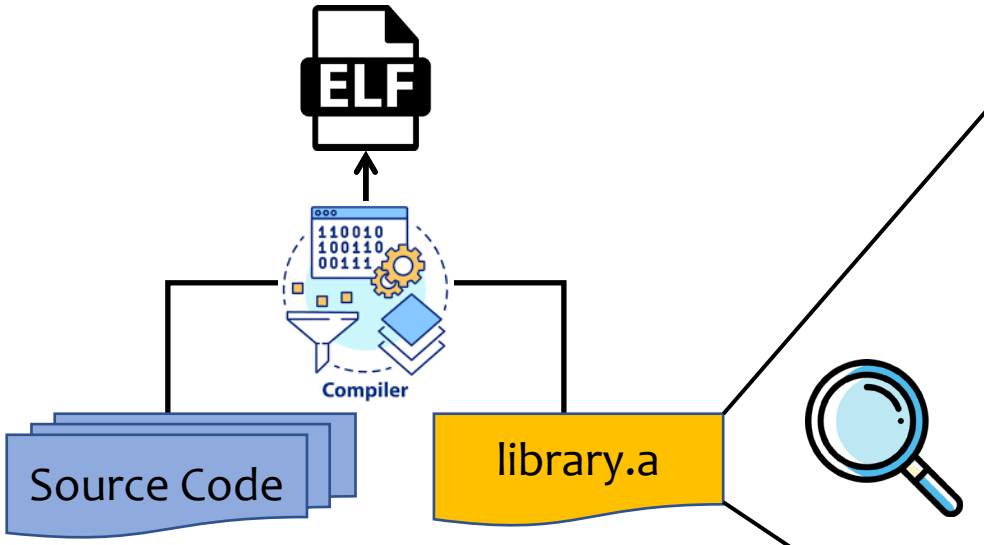

Compilation phase

API	Description
void *sa_alloc(size_t *length*, bool *need_ro*, long **offset*);	Allocate an isolated U-page region at the page granularity. If specified, it also allocates a shared isolated S-page region.
bool sa_free(void **addr*, size_t *length*);	Free an isolated U-page region with the specified length.
#define SWITCH_IN \ asm("stac\n");	Disable SMAP—access the isolated U-page region is allowed.
#define SWITCH_OUT \ asm("clac\n");	Enable SMAP—access to the isolated U-page region is denied.

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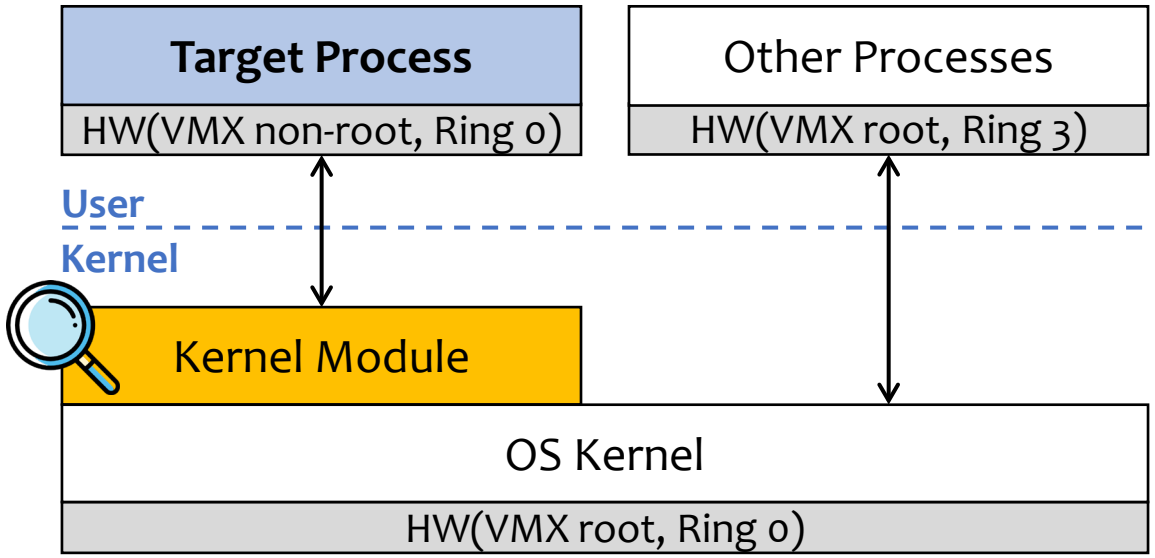

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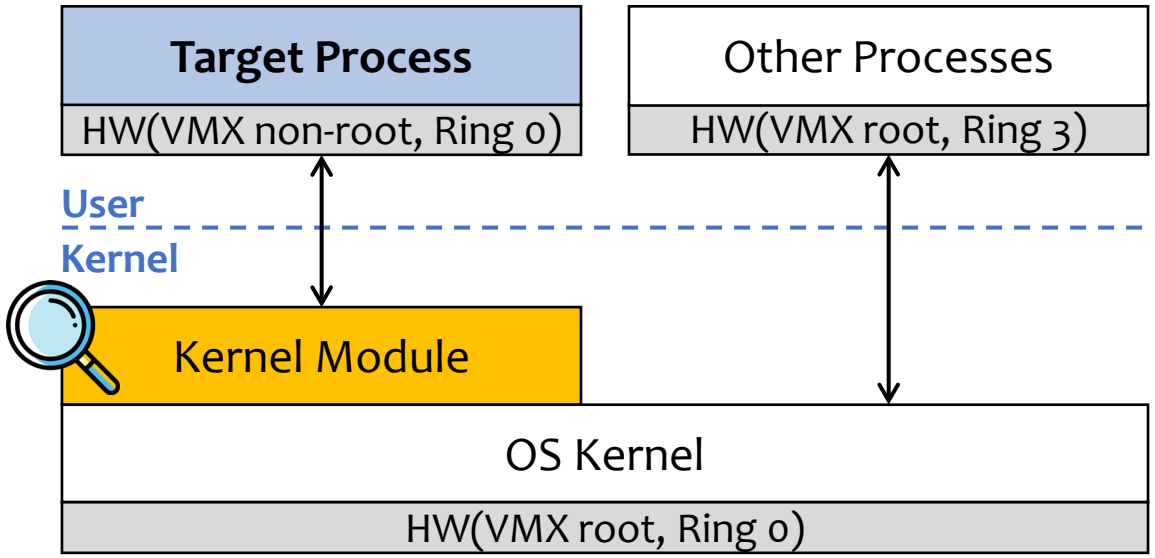

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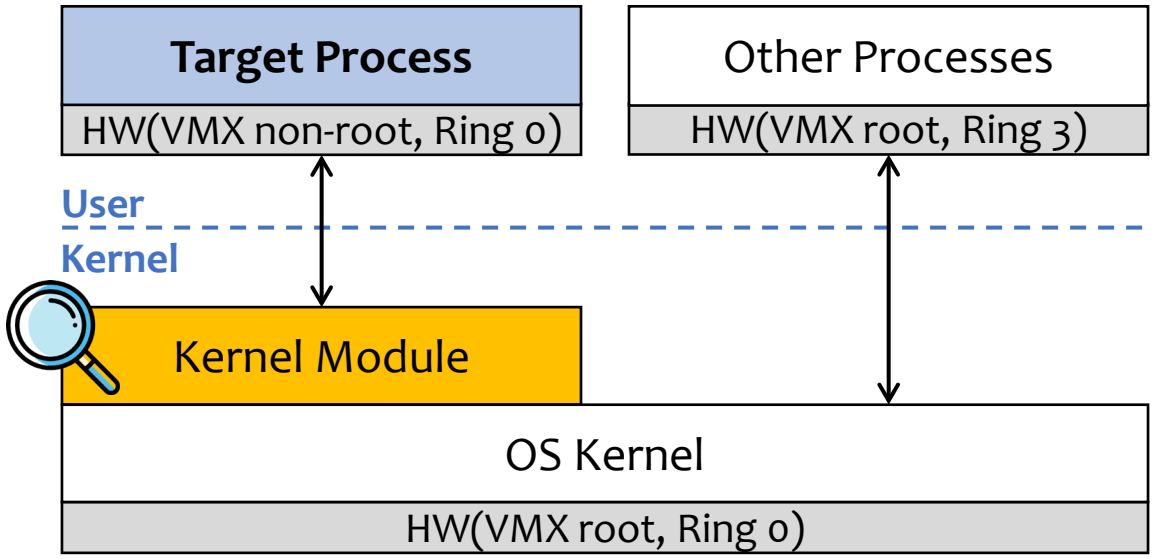

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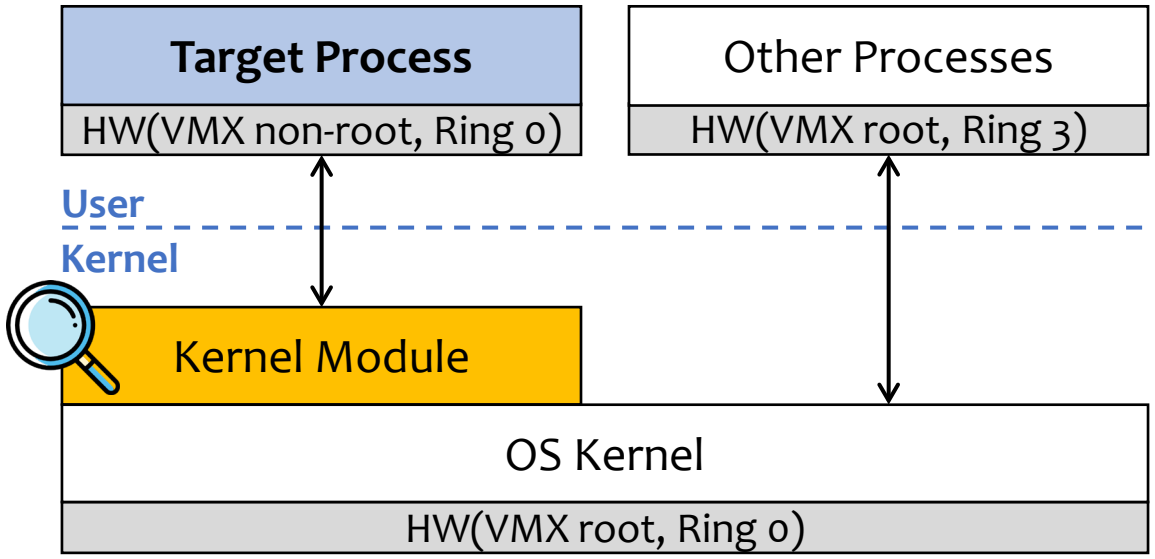

Runtime Phase

3 Events Redirection Component

– Handles system calls, interrupts, exceptions, and Linux signals.

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  - The guest/host page-tables share the last three-level page table entries.
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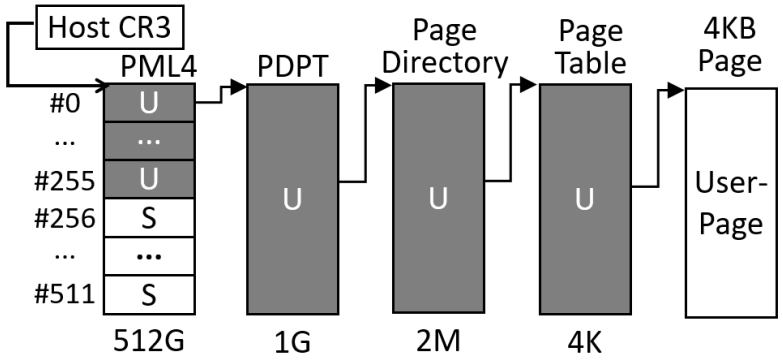

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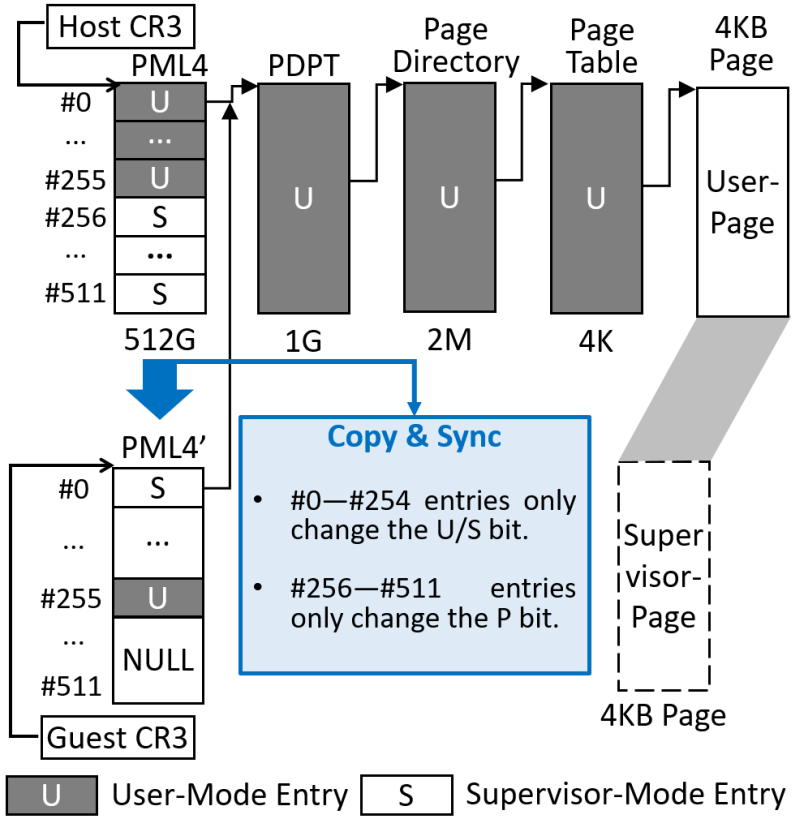

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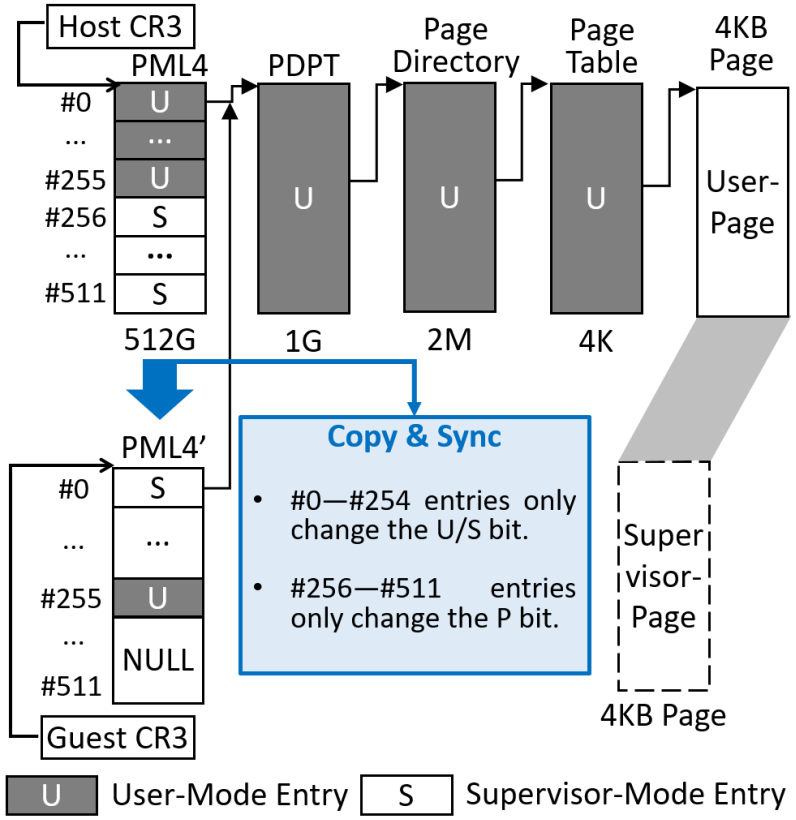

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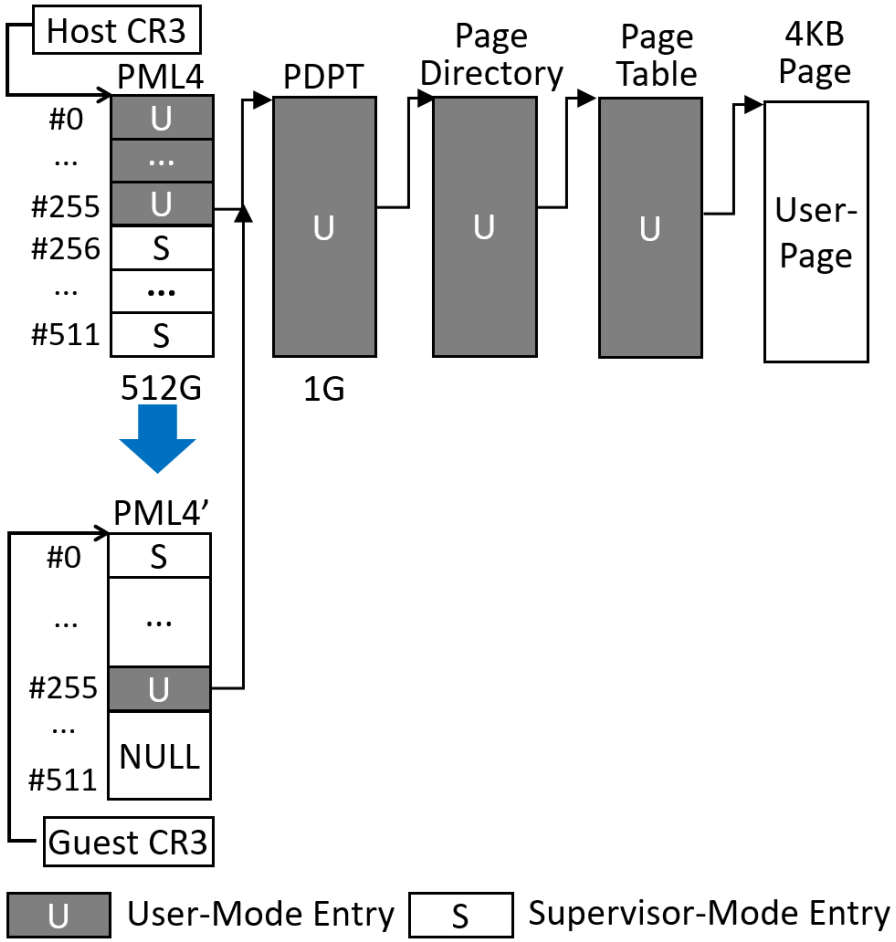

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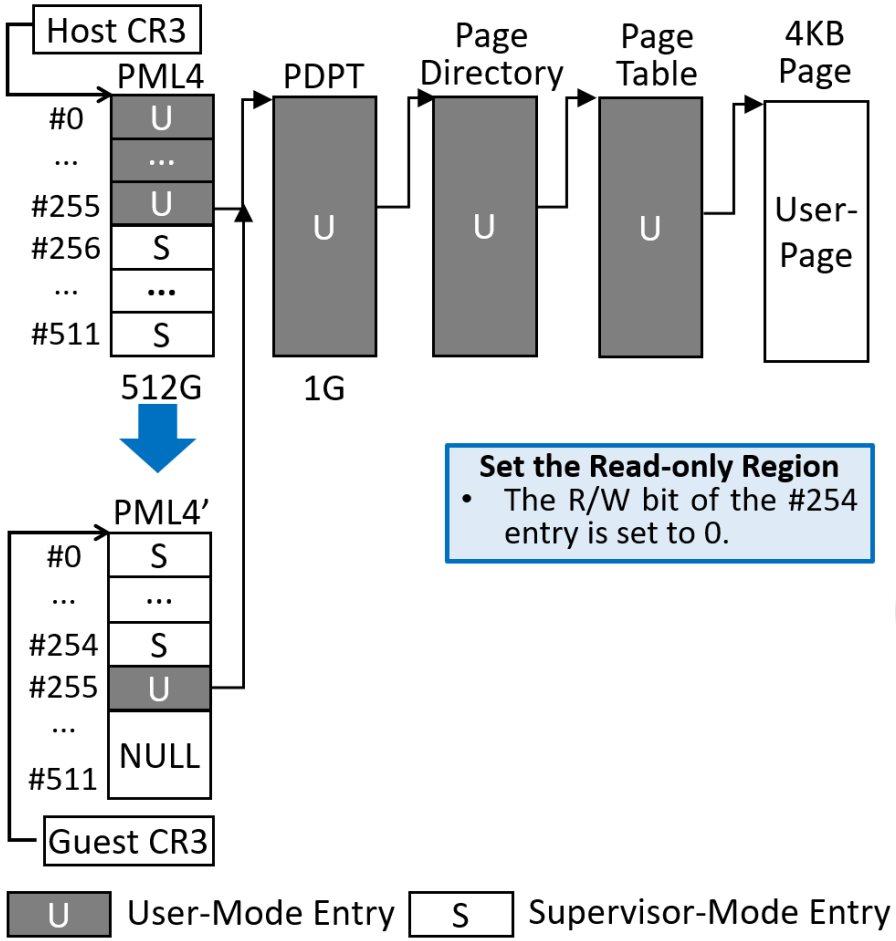

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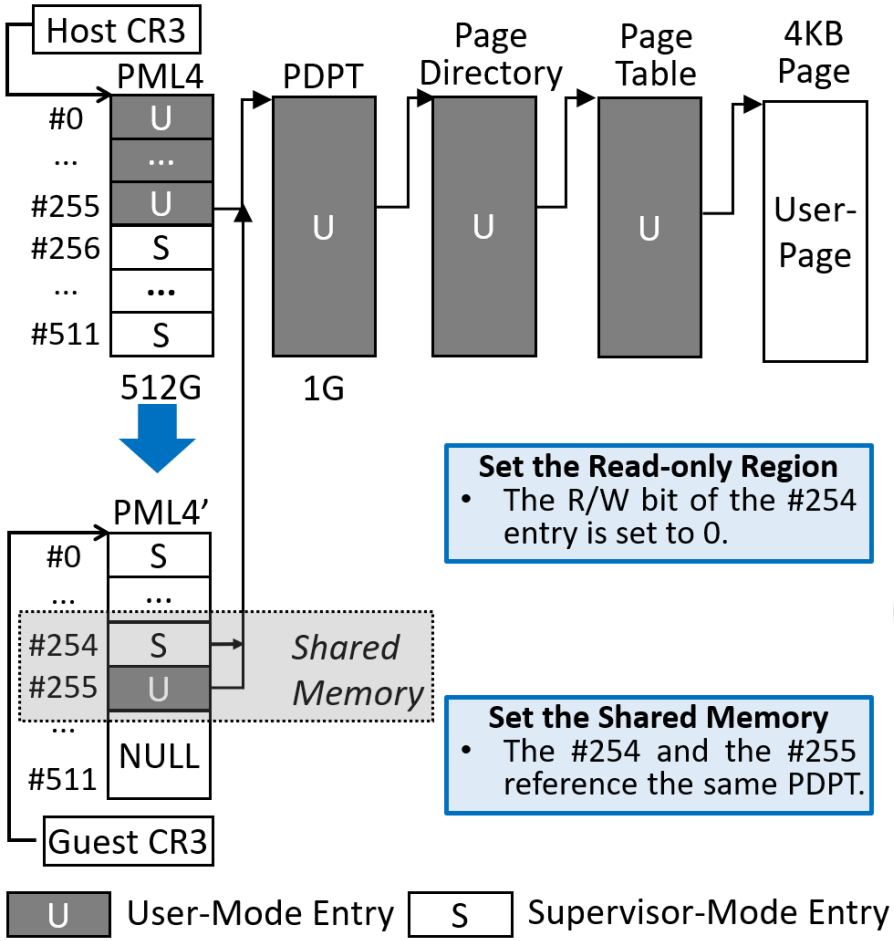

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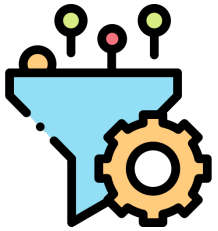
2 Manual Verification

- We **manually** review the description of all X86 instructions by reading the Intel Software Developers' Manual.
- Confirm the first step is **complete**, and also find the instructions that **behave differently in ring 0 and ring 3.**

SEIMI —— Privileged Instruction Prevention Component

- We group them into **20 categories** based on their different functionality.



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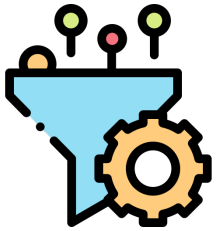

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2	INVD. XSETBV	Y
3	ENCLS(e.g., ECREATE, EADD, EINIT, EDBGRD…)	Y
4	RDMSR, WRMSR	Y
5	IN, OUT, IN[S|SB|SW|SD], OUT[S|SB|SW|SD]	Y
6	HLT, INVLPG, RDPMC, MONITOR, MWAIT, WBINVD	Y
7	LGDT, LLDT, LTR, LIDT	Y
8	MOV to/from DR0-DR7	Y
9	MOV to/from CR3, MOV to/from CR8	Y
10	MOV to/from CR0/CR4, CLTS, LMSW, SMSW	Y
11	MOV to/from CR2	Y
12	SWAPGS	Y
13	CLI, STI	Y
14	LAR, LSL. VERR, VERW	N
15	POPF, POPFQ	N
16	L[FS|DS|SS], MOV to [DS|ES|FS|GS|SS], POP [FS|GS]	N
17	Far CALL, Far RET, Far JMP	N
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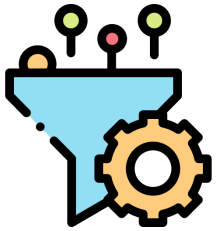

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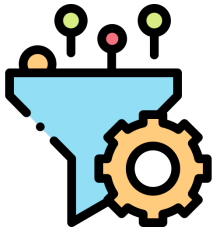

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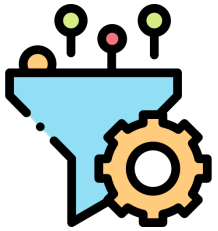

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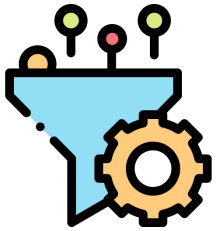

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3 **Raising the #GP (general protection exception)**

– Segment-switching related instructions: mov to %ds, lcall…

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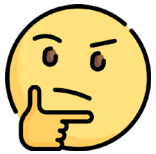

How to intercept this type of instructions ???

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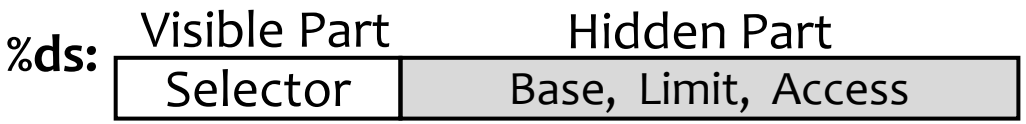
- **Segment-switching exception using descriptor cache.**



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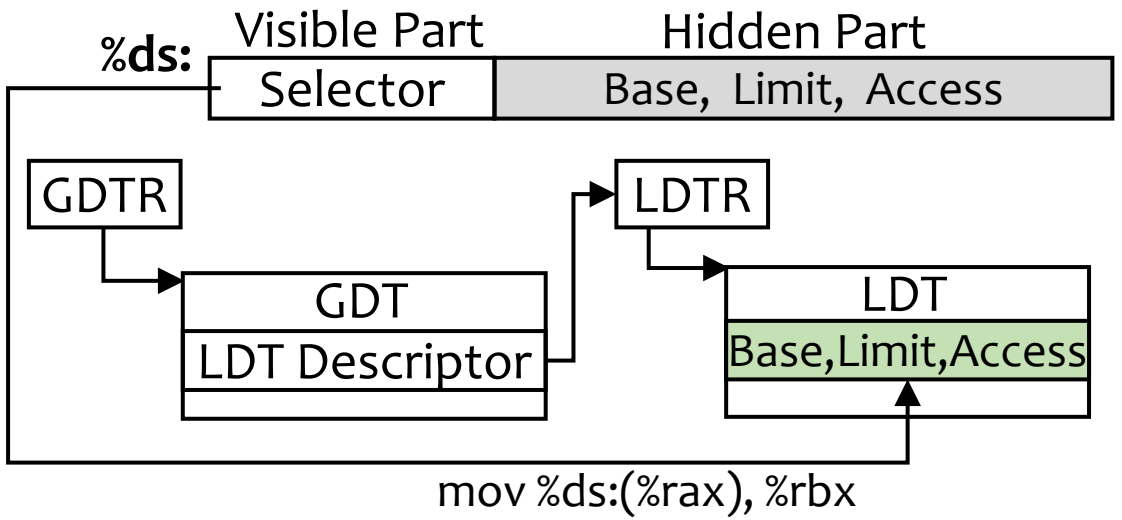

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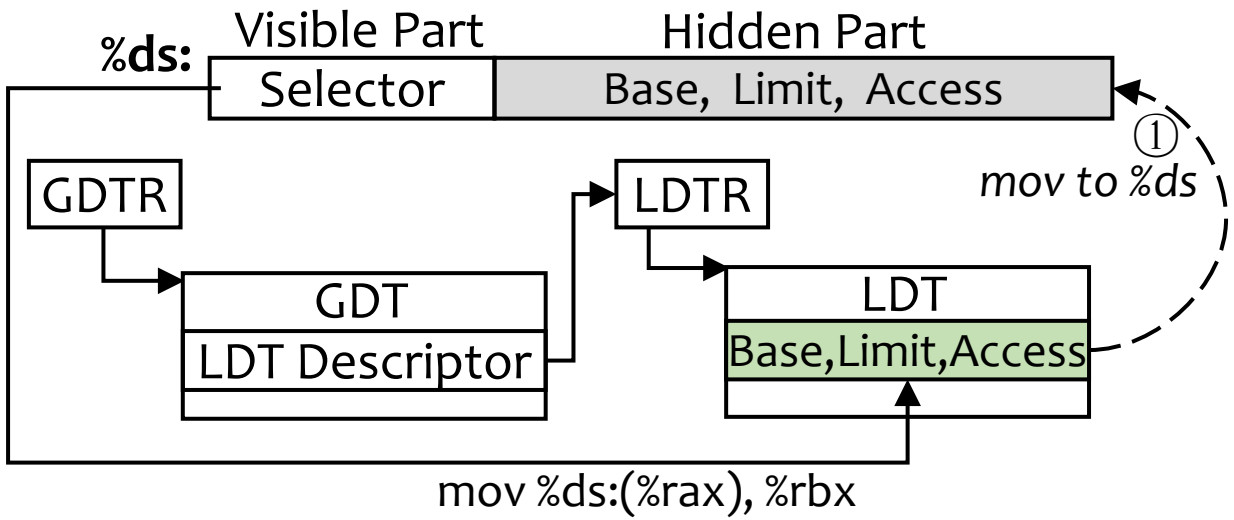

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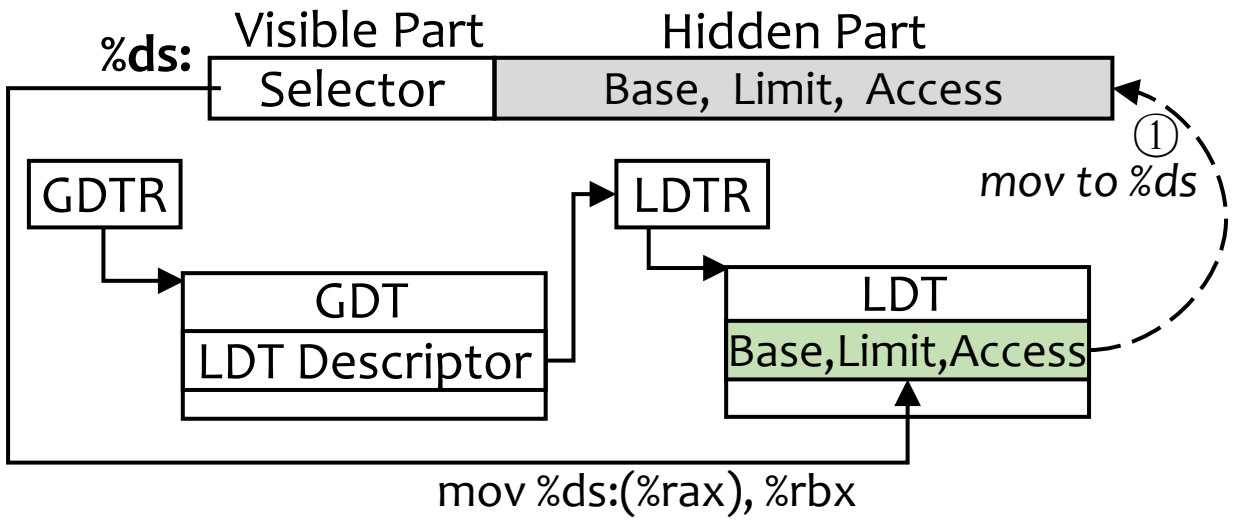

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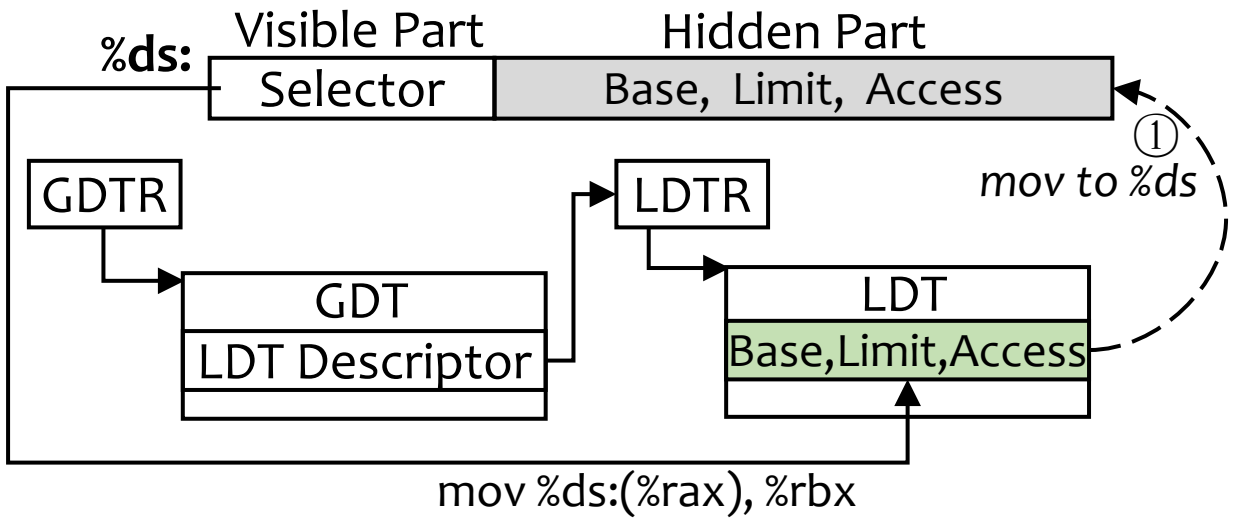

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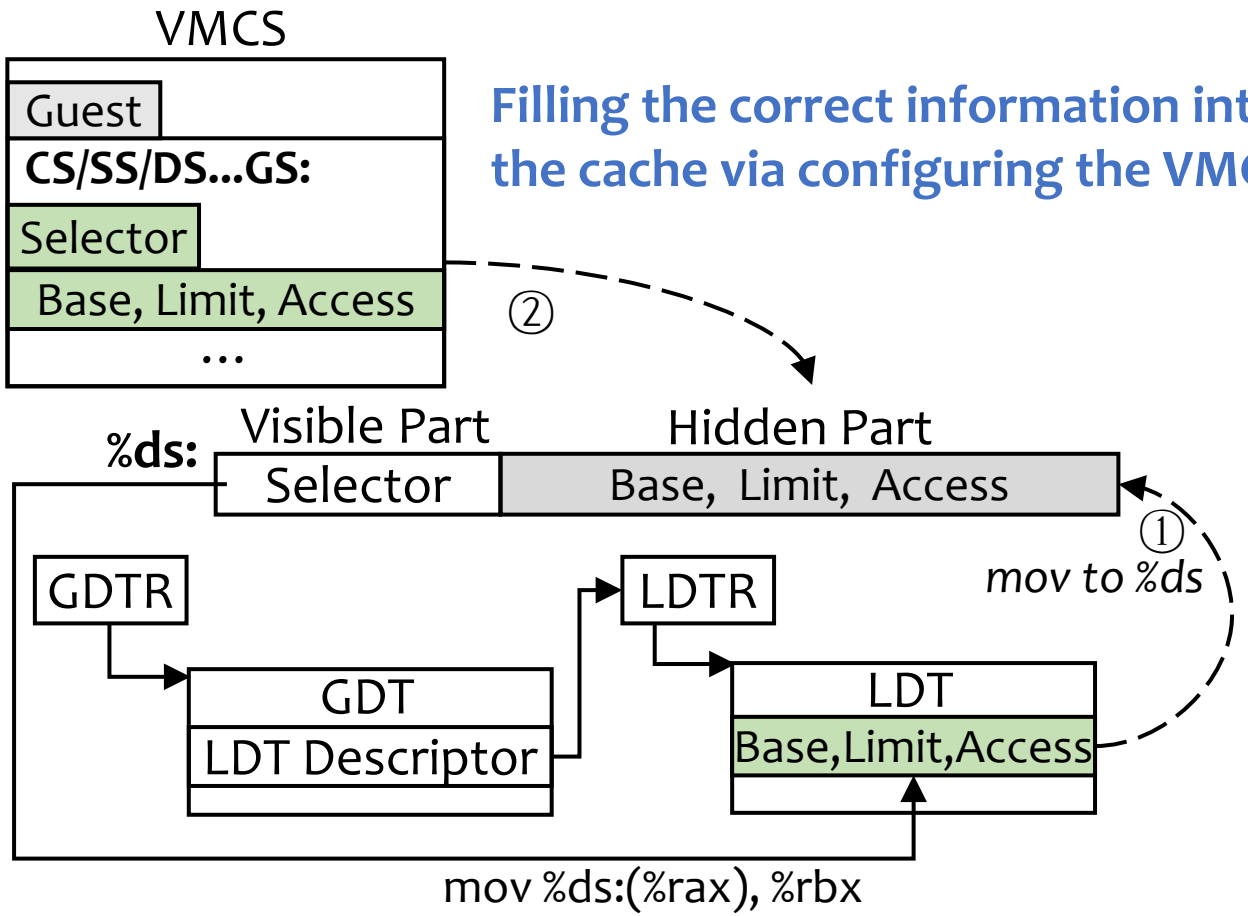

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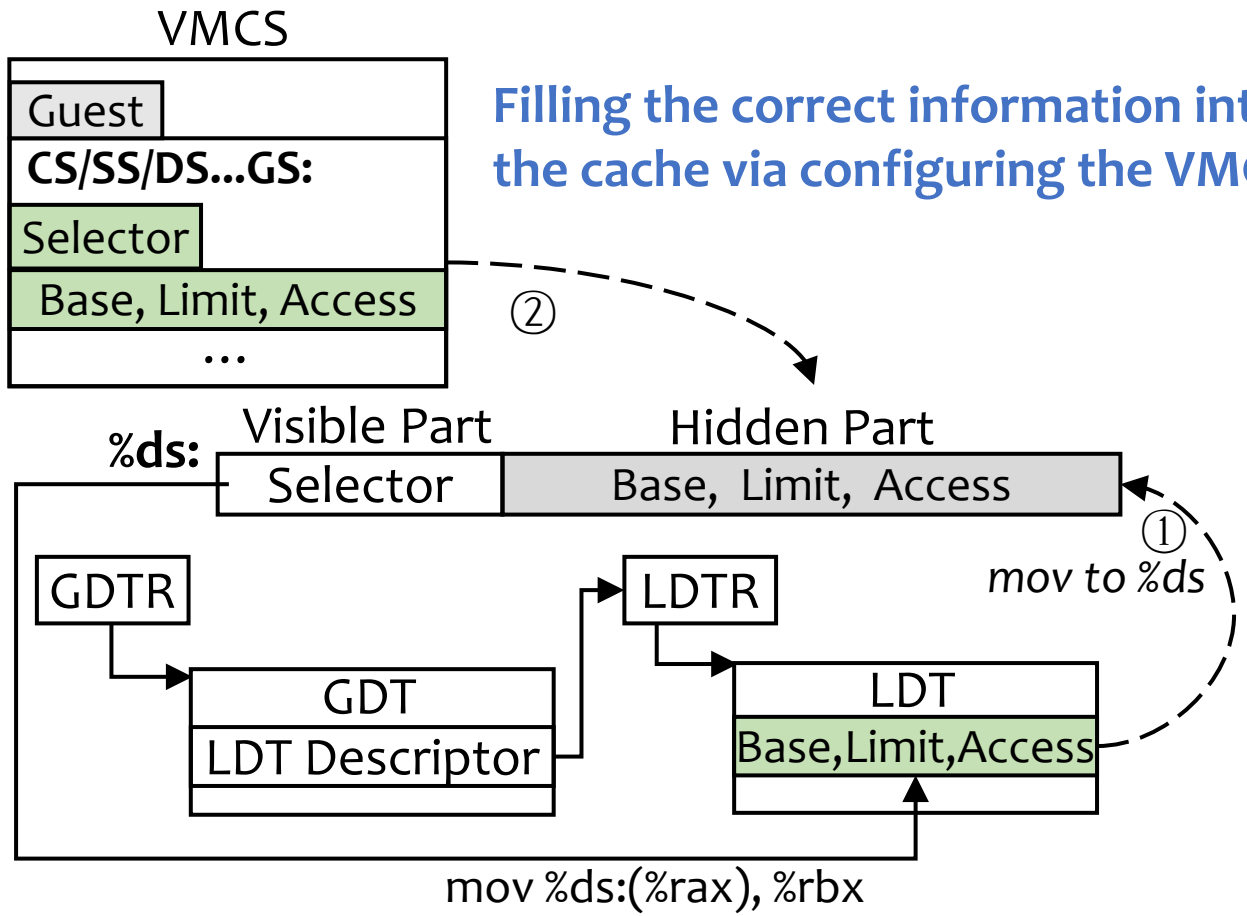

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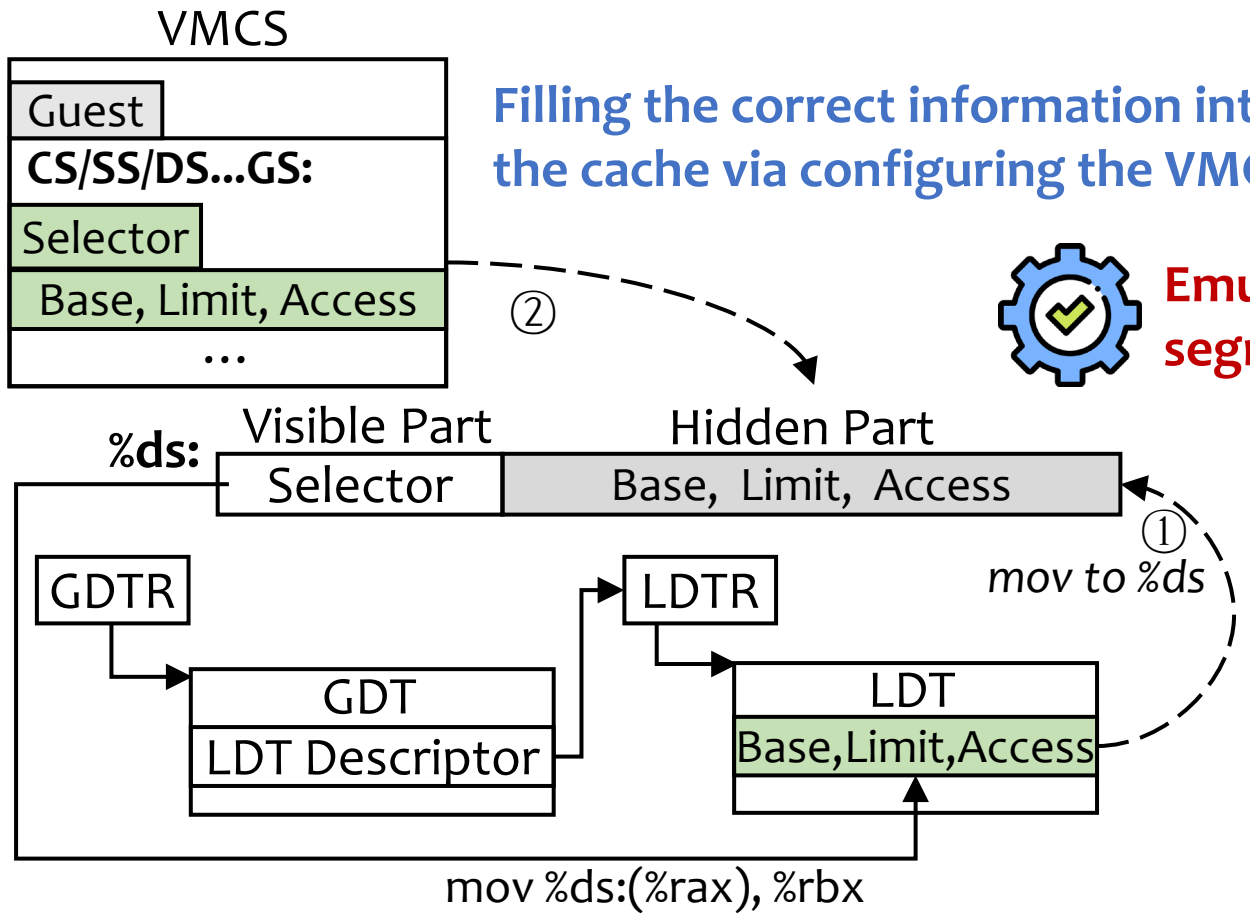

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- **SWAPGS, L[AR/SL], VER[R/W], CLI/STI …**
  - More details are in the paper.🔍

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  - Convert the system calls to the hypercalls via mapping a code page.
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  - Check the signal queue, and switch the context via configuring the VMCS.

SEIMI —— Some Implementations

- **Memory Management Implementations**
  - Avoiding overlaps in the 254th and 255th entries.
  - Handling the VSYSCALL page.
  - Tracking updates of the PML4 page.
  - Avoiding accessing the kernel by exploiting the TLB.

- **Other Implementations**
  - Hardening system calls against confused deputy.
  - Starting and exiting the target process.
  - Supporting multi-threading and multi-processes.
  - Defeating the concurrent attacks.

SEIMI: Efficient and Secure SMAP-Enabled Intra-process Memory Isolation

Zhe Wang[1,2] Chenggang Wu[1,2] Mengyao Xie[1,2] Yinqian Zhang[3] Kangjie Lu[4]
Xiaofeng Zhang[1,2] Yuanming Lai[1,2] Yan Kang[1] Min Yang[5]

[1] *State Key Laboratory of Computer Architecture, Institute of Computing Technology, Chinese Academy of Sciences,*
[2] *University of Chinese Academy of Sciences,* [3] *The Ohio State University,* [4]*University of Minnesota,* [5]*Fudan University*

***Abstract*—Memory-corruption attacks such as code-reuse attacks and data-only attacks have been a key threat to systems security. To counter these threats, researchers have proposed a variety of defenses, including *control-flow integrity* (CFI), *code-pointer integrity* (CPI), and code (re-)randomization. All of them, to be effective, require a security primitive—intra-process protection of confidentiality and/or integrity for sensitive data (such as CFI's shadow stack and CPI's safe region).**

In this paper, we propose SEIMI, a highly efficient intra-process memory is[illegible]nique for memory-corruption defenses to prot[illegible]ata. The core of SEIMI is to use the c[illegible] *Access Prevention (SMAP)*, a hardwar[illegible] used for preventing the kernel fr[illegible] to achieve intra-process memory i[illegible]EIMI creatively executes the user c[illegible] addition to enabling the new desig[illegible]ry isolation, we further develop mi[illegible]nsure secure escalation of user code, e.[illegible]es to capture the potential segment operat[illegible]*irtual Machine Control Structure* (VMCS) [illegible] result of the control registers related operations. Exten[illegible]tal results show that SEIMI outperforms existing isola[illegible]ms, including both the *Memory Protection Keys* (M[illegible] scheme and the *Memory Protection Extensions* (MPX[illegible]scheme, while providing secure memory isolation.

I. Introduction

Memory-corruption attacks such as control-flow hijacking and data-only attacks have been a major threat to systems security in the past decades. To defend against such attacks, researchers have proposed a variety of advanced mechanisms, including enhanced control-flow integrity (CFI), code-pointer integrity (CPI), fine-grained code (re-)randomization, and data-layout randomization. All these techniques require a security primitive—effective intra-process memory protection of the integrity and/or confidentiality of sensitive data from potentially compromised code. The sensitive data includes critical data structures that are frequently checked against or used for protection. For example, O-CFI [39] uses a *bounds lookup table* (BLT), and CCFIR [58] uses a *safe SpringBoard* to restrict the control flow; CPI [31] uses a *safe region*, and Shuffler [55] uses a *code-pointer table* to protect the sensitive pointers; Oxymoron [6] maintains a *sensitive translation table*, and Isomeron [19] uses a table to protect randomization secrets. The effectiveness of all such techniques heavily depends on the integrity and/or confidentiality of the sensitive data.

To efficiently protect sensitive data, researchers proposed *information hiding* (IH) which stores sensitive data in a memory region allocated in a *random* address and wishes that attackers could not know the random address thus could not write or read the sensitive data. Unfortunately, recent works show that memory disclosures and side channels can be exploited to readily reduce the randomization entropy and thus to bypass the information hiding [22–24, 36, 41]. As such, even a robust IH-based defense can be defeated.

To address this problem, recent research instead opts for *practical memory isolation* which provides efficient protection with a stronger security guarantee. Memory isolation, in general, can be classified into *address-based* isolation and *domain-based* isolation. Address-based isolation checks (e.g., bound-check) *each* memory access from untrusted code to ensure that it cannot access the sensitive data. The main overhead of this method is brought by the code that performs the checks. The most efficient address-based isolation is based on Intel Memory Protection Extensions (MPX), which performs bound-checking with hardware support [30].

Domain-based isolation instead stores sensitive data in a protected memory region. The permission to accessing this region is granted when requested by the trusted code, and is revoked when the trusted access finished. However, memory accesses from untrusted code (i.e., the potentially vulnerable code that can be compromised by attackers) cannot enable the permission. The main source of the performance overhead of domain-based memory isolation is the operations for enabling and disabling the memory-access permissions. The most efficient domain-based isolation is to use Intel Memory Protection Keys (MPK) [25, 30, 40, 47].

In general, existing address-based isolation and domain-based isolation both incur non-trivial performance overhead compared to the IH-based scheme. Worse, the overhead will be significantly elevated when the workloads (i.e., the frequency of memory accesses that require bound-checking or permission switching) increase. For example, when protecting the shadow stack, the MPK-based scheme (i.e., domain-based) incurs a runtime overhead of 61.18% [40]. When protecting the safe region of CPI using the MPX-based scheme (i.e., address-

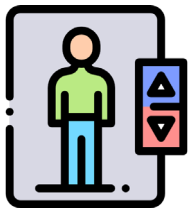
Outline

Motivation

High-level Design

Approach Overview

SEIMI System



Evaluation

Performance Evaluation

- **Defenses and Isolation Schemes:**
  - Defenses: O-CFI, Shadow Stack (SS), Code Pointer Integrity (CPI), and ASLR-Guard (AG)
  - Isolation: IH-based (randomization), MPX-based, MPK-based, and SEIMI-based schemes

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- **Real-world applications:**
  - 4 Web servers: Nginx, Apache, Lighttpd, and Openlitespeed.
  - 4 Databases: MySQL, SQLite, Redis, and Memcached.
  - 4 JavaScript engines: ChakraCore, Google V8, JavaScriptCore, SpiderMonkey.

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Config	null call	null I/O	stat	open close	select TCP	signal install	signal handle	fork proc	exec proc	sh proc
Native	0.21	0.26	0.57	1.23	5.35	0.27	0.99	355	870	2162
SEIMI	**0.71**	**0.82**	**1.33**	**2.58**	6.11	**0.79**	**3.02**	463	1029	2368
Slowdown	**2.4X**	**2.2X**	**1.3X**	**1.1X**	14%	**1.9X**	**2.1X**	30.4%	18.3%	9.5%

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Slowdown	20.0%	18.9%	16.1%	24.2%	21.3%	36.7%	26.2%

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SEIMI	6.9623	5.3421	14.5	7.4527	12500	1.038	0.2128	1.705
Slowdown	27.2%	11.7%	33.0%	12.6%	84.4%	63.2%	33.6%	67.8%

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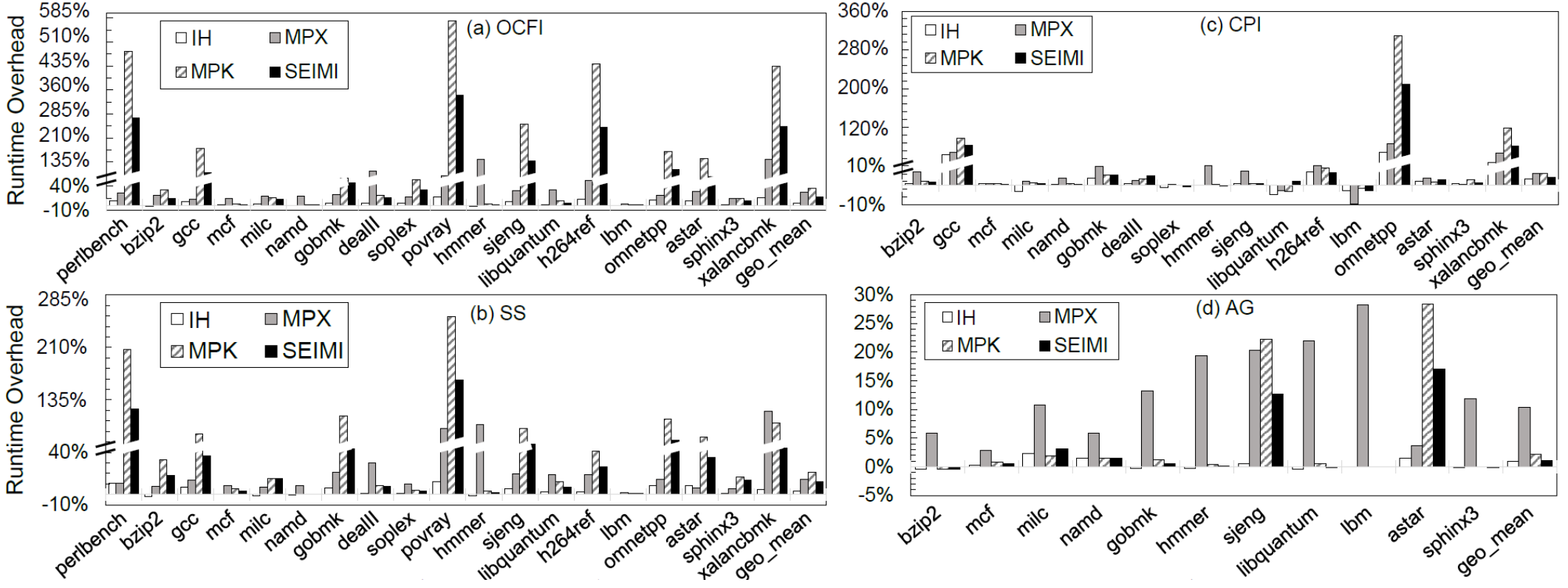
Config	Pipe	AF UNIX	UDP	RPC/ UDP	TCP	RPC/ TCP	TCP conn
Native	5.582	9.2	9.883	14.9	13.9	17.6	22
SEIMI	7.428	11.7	11.7	20	17.6	23.9	24
Slowdown	33.1%	27.2%	18.4%	34.2%	26.6%	35.8%	9.1%

4 Local-communication latency (in µs): smaller is better.

Macrobenchmark —— SPEC CPU 2006 benchmark

- Compared with the **MPX-based scheme**, **SEIMI** achieves a lower performance overhead on average, with the average reduction of **33.97%**.



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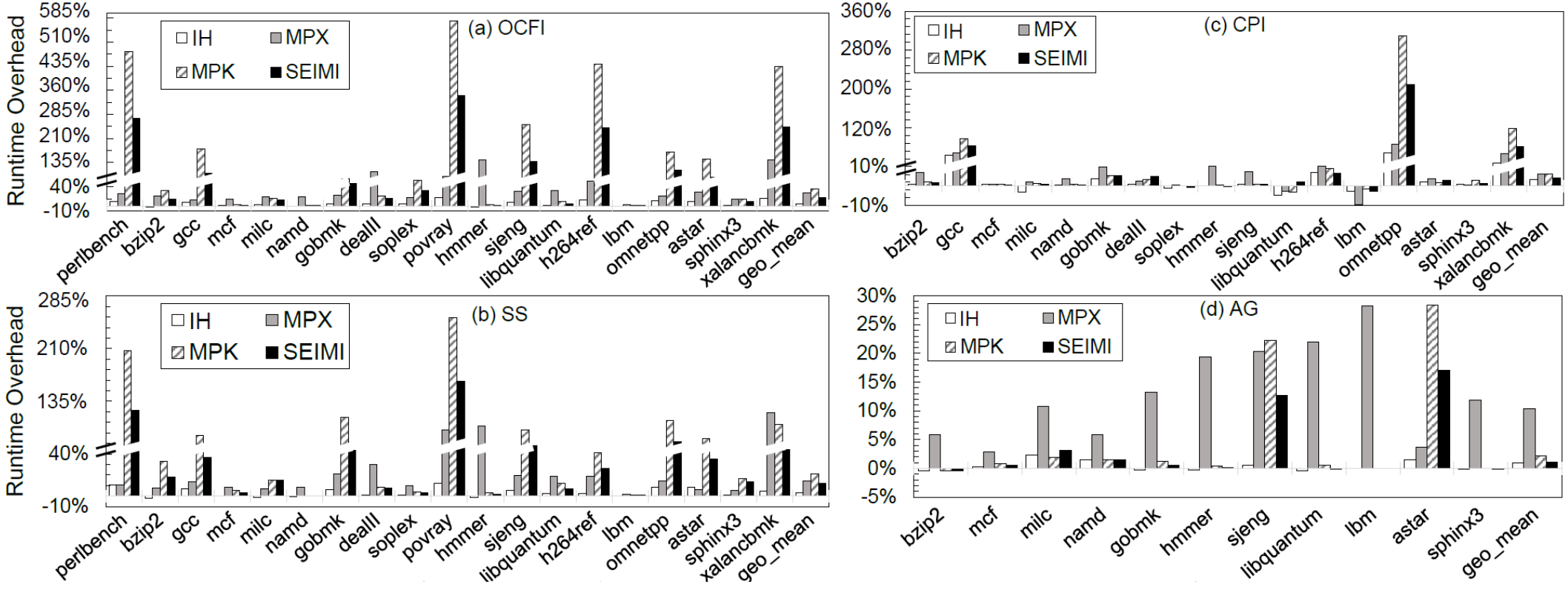
- Compared with the **MPX-based scheme**, **SEIMI** achieves a lower performance overhead on average, with the average reduction of **33.97%**.
- Compared to the **MPK-based scheme**, **SEIMI** is more efficient in almost all test cases, and with the average reduction of **42.3%** (maximum is **133.33%**).



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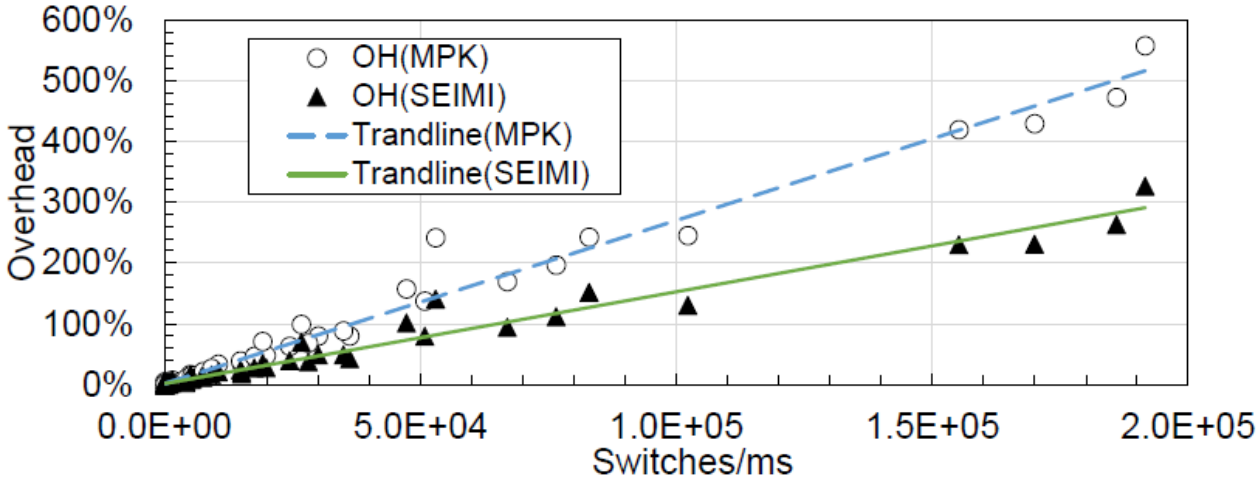

The impact of permission-switching frequency on performance of MPK and SEIMI.

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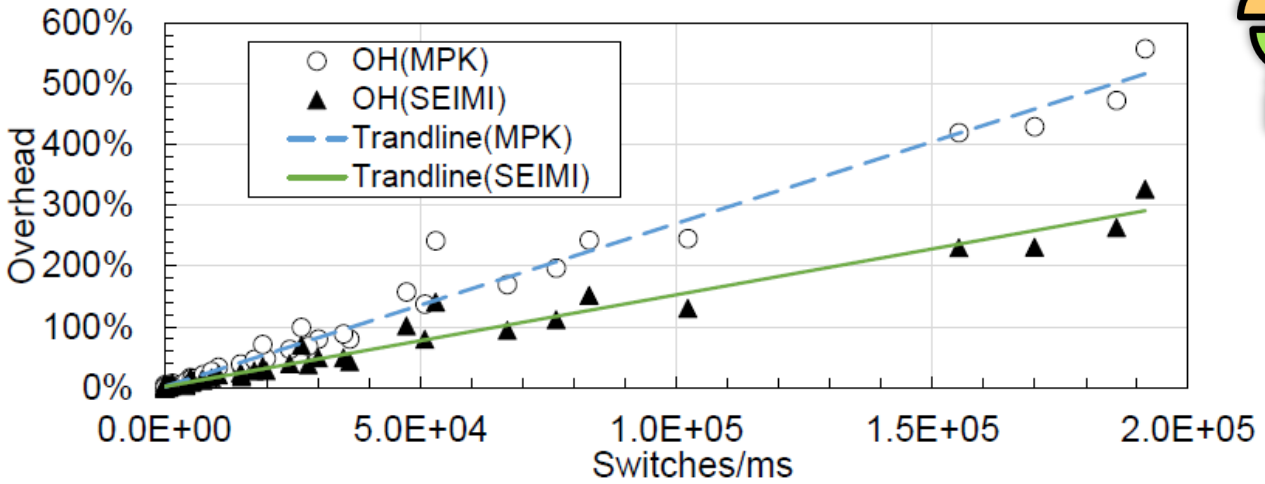
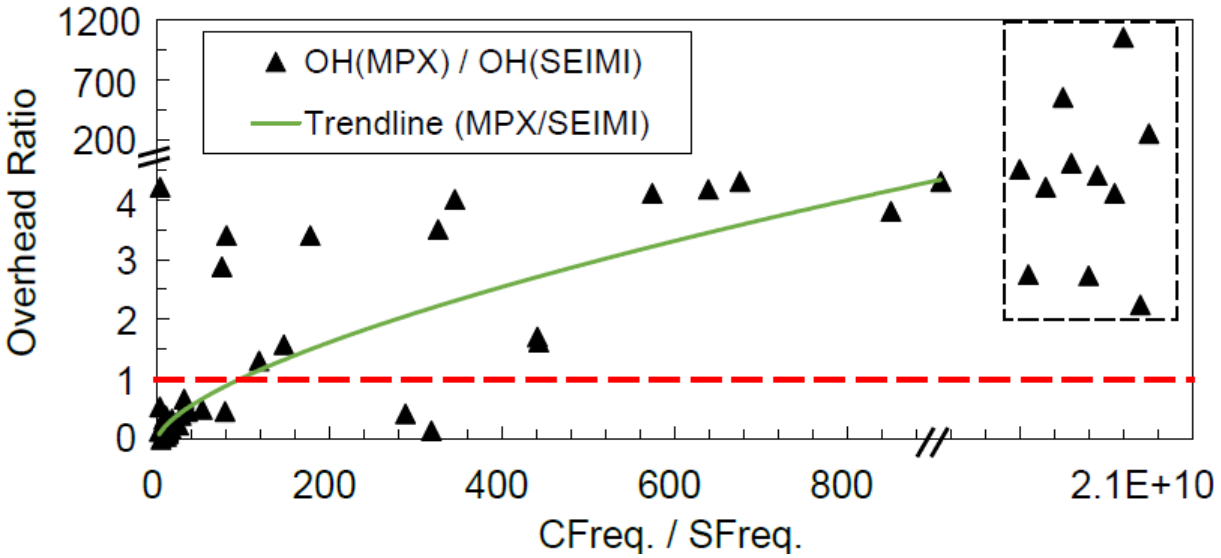


The impact of permission-switching frequency on performance of MPK and SEIMI.

Compared to **MPK**, as the access permission switching frequency increases, the performance gain of **SEIMI** becomes more apparent.

Macrobenchmark —— SPEC CPU 2006 benchmark

- **Performance Analysis: MPX vs. SEIMI**



The impact of bound-checking frequency (CFreq) and permission-switching frequency (SFreq) on performance.

Macrobenchmark —— SPEC CPU 2006 benchmark

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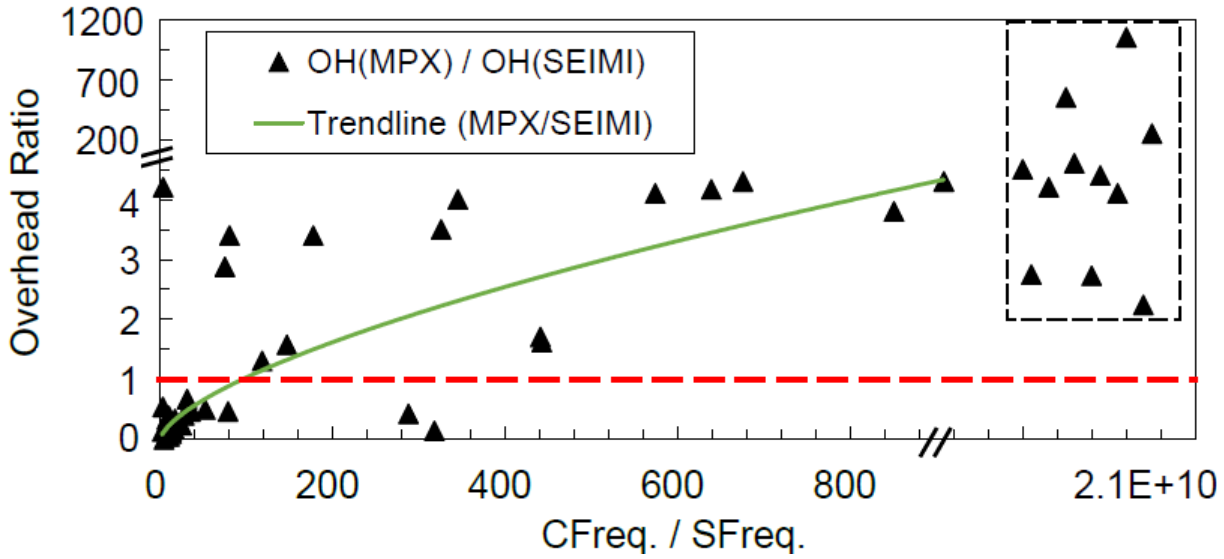

When the bound-checking frequency is **52** times of the access permission switching frequency, **SEIMI** is more efficient than **MPX** in most cases.

The impact of bound-checking frequency (CFreq) and permission-switching frequency (SFreq) on performance.

Real-world Applications

- **SEIMI is more performant than MPX-based and MPK-based schemes on protecting the real-world applications.**

Applications	OCFI				SS				CPI				AG			
	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI
Nginx	1.10%	3.86%	5.32%	1.77%	1.86%	7.33%	10.49%	2.43%	0.90%	6.38%	8.95%	3.08%	0.74%	7.60%	5.27%	2.01%
Apache	1.58%	4.71%	2.82%	1.82%	1.64%	6.36%	6.83%	2.15%	1.45%	5.01%	2.58%	1.80%	—	—	—	—
Lighttpd	**2.94%**	**3.42%**	**5.74%**	**4.46%**	2.77%	6.85%	6.33%	3.78%	1.70%	6.83%	3.42%	2.46%	—	—	—	—
Openlitespeed	1.44%	5.39%	3.88%	1.61%	1.04%	1.92%	3.39%	1.42%	0.91%	2.89%	2.99%	1.38%	—	—	—	—
MySQL	1.75%	12.09%	8.08%	3.79%	3.17%	9.60%	11.99%	3.94%	—	—	—	—	—	—	—	—
SQLite	1.61%	2.11%	2.70%	1.84%	1.42%	3.46%	2.19%	1.94%	1.36%	3.11%	2.66%	2.18%	—	—	—	—
Redis	**4.51%**	**5.46%**	**13.12%**	**10.31%**	**1.18%**	**2.81%**	**5.36%**	**5.06%**	1.24%	4.47%	4.81%	3.93%	—	—	—	—
Memcached	1.64%	6.64%	7.46%	2.74%	2.38%	5.57%	8.13%	3.44%	1.04%	6.02%	7.28%	1.60%	—	—	—	—
ChakraCore	3.03%	12.09%	9.90%	4.10%	4.37%	7.92%	10.09%	5.15%	—	—	—	—	—	—	—	—
V8	2.57%	11.63%	5.04%	3.37%	2.05%	8.01%	4.05%	2.96%	—	—	—	—	—	—	—	—
JavaScriptCore	**2.22%**	**22.87%**	**39.65%**	**26.81%**	20.69%	38.34%	47.77%	31.82%	—	—	—	—	—	—	—	—
SpiderMonkey	1.75%	9.32%	7.63%	4.15%	1.84%	7.56%	7.79%	5.19%	—	—	—	—	—	—	—	—

All overheads are normalized to the unprotected applications. "—" represents the defense failed to compile or run it.

Real-world Applications

- **SEIMI is more performant than MPX-based and MPK-based schemes on protecting the real-world applications.**
  - SEIMI is much more efficient than MPK for all 32 cases.

Applications	OCFI				SS				CPI				AG			
	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI
Nginx	1.10%	3.86%	5.32%	1.77%	1.86%	7.33%	10.49%	2.43%	0.90%	6.38%	8.95%	3.08%	0.74%	7.60%	5.27%	2.01%
Apache	1.58%	4.71%	2.82%	1.82%	1.64%	6.36%	6.83%	2.15%	1.45%	5.01%	2.58%	1.80%	—	—	—	—
Lighttpd	**2.94%**	**3.42%**	**5.74%**	**4.46%**	2.77%	6.85%	6.33%	3.78%	1.70%	6.83%	3.42%	2.46%	—	—	—	—
Openlitespeed	1.44%	5.39%	3.88%	1.61%	1.04%	1.92%	3.39%	1.42%	0.91%	2.89%	2.99%	1.38%	—	—	—	—
MySQL	1.75%	12.09%	8.08%	3.79%	3.17%	9.60%	11.99%	3.94%	—	—	—	—	—	—	—	—
SQLite	1.61%	2.11%	2.70%	1.84%	1.42%	3.46%	2.19%	1.94%	1.36%	3.11%	2.66%	2.18%	—	—	—	—
Redis	**4.51%**	**5.46%**	**13.12%**	**10.31%**	**1.18%**	**2.81%**	**5.36%**	**5.06%**	1.24%	4.47%	4.81%	3.93%	—	—	—	—
Memcached	1.64%	6.64%	7.46%	2.74%	2.38%	5.57%	8.13%	3.44%	1.04%	6.02%	7.28%	1.60%	—	—	—	—
ChakraCore	3.03%	12.09%	9.90%	4.10%	4.37%	7.92%	10.09%	5.15%	—	—	—	—	—	—	—	—
V8	2.57%	11.63%	5.04%	3.37%	2.05%	8.01%	4.05%	2.96%	—	—	—	—	—	—	—	—
JavaScriptCore	**2.22%**	**22.87%**	**39.65%**	**26.81%**	20.69%	38.34%	47.77%	31.82%	—	—	—	—	—	—	—	—
SpiderMonkey	1.75%	9.32%	7.63%	4.15%	1.84%	7.56%	7.79%	5.19%	—	—	—	—	—	—	—	—

All overheads are normalized to the unprotected applications. "—" represents the defense failed to compile or run it.

Real-world Applications

- **SEIMI is more performant than MPX-based and MPK-based schemes on protecting the real-world applications.**
  - SEIMI is much more efficient than MPK for all 32 cases.
  - SEIMI is much more efficient than MPX for 28 cases.

Applications	OCFI				SS				CPI				AG			
	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI	IH	MPX	MPK	SEIMI
Nginx	1.10%	3.86%	5.32%	1.77%	1.86%	7.33%	10.49%	2.43%	0.90%	6.38%	8.95%	3.08%	0.74%	7.60%	5.27%	2.01%
Apache	1.58%	4.71%	2.82%	1.82%	1.64%	6.36%	6.83%	2.15%	1.45%	5.01%	2.58%	1.80%	—	—	—	—
Lighttpd	**2.94%**	**3.42%**	**5.74%**	**4.46%**	2.77%	6.85%	6.33%	3.78%	1.70%	6.83%	3.42%	2.46%	—	—	—	—
Openlitespeed	1.44%	5.39%	3.88%	1.61%	1.04%	1.92%	3.39%	1.42%	0.91%	2.89%	2.99%	1.38%	—	—	—	—
MySQL	1.75%	12.09%	8.08%	3.79%	3.17%	9.60%	11.99%	3.94%	—	—	—	—	—	—	—	—
SQLite	1.61%	2.11%	2.70%	1.84%	1.42%	3.46%	2.19%	1.94%	1.36%	3.11%	2.66%	2.18%	—	—	—	—
Redis	**4.51%**	**5.46%**	**13.12%**	**10.31%**	**1.18%**	**2.81%**	**5.36%**	**5.06%**	1.24%	4.47%	4.81%	3.93%	—	—	—	—
Memcached	1.64%	6.64%	7.46%	2.74%	2.38%	5.57%	8.13%	3.44%	1.04%	6.02%	7.28%	1.60%	—	—	—	—
ChakraCore	3.03%	12.09%	9.90%	4.10%	4.37%	7.92%	10.09%	5.15%	—	—	—	—	—	—	—	—
V8	2.57%	11.63%	5.04%	3.37%	2.05%	8.01%	4.05%	2.96%	—	—	—	—	—	—	—	—
JavaScriptCore	**2.22%**	**22.87%**	**39.65%**	**26.81%**	20.69%	38.34%	47.77%	31.82%	—	—	—	—	—	—	—	—
SpiderMonkey	1.75%	9.32%	7.63%	4.15%	1.84%	7.56%	7.79%	5.19%	—	—	—	—	—	—	—	—

All overheads are normalized to the unprotected applications. "—" represents the defense failed to compile or run it.

Conclusion

- **We propose a highly efficient intra-process memory isolation technique SEIMI, which leverages the widely used hardware feature — SMAP.**

- **To avoid introducing security threats, we propose multiple new techniques to ensure the user code run in ring 0 securely.**

- **We believe that SEIMI can not only benefit existing defenses, but also open the new research direction …**
  - Enabling the efficient access to a variety of privileged hardware features, which does not require context switch, to defenses.

Any Questions ?

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